The Logic Visualiser

Usage

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Circuit Description

For the official kit from

OmberTech

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Introduction

This booklet details information valuable to the constructor, user, and even curious bystander of the Logic Visualiser kit by OmberTech.

The Logic Visualiser is designed as a simpler, smaller, (to say nothing of cheaper) alternative to a logic analyser. It displays the logic states of sixteen TTL or CMOS inputs between 3 and 18 Volts, either sampled regularly to show the real−time logic state of slow signals, or with a configurable delay to allow analysis of signals changing faster than the eye can see. In this latter case, a further facility is provided for viewing repeating clocked signals, this samples the inputs exactly one clock pulse after the previous display and thereby allows even fast changing signals to be observed in sequence.

A further function is to sample 127 bits of clocked data at a selected pin, then repeatedly display that data at an adjustable, pausable, rate on the sixteen input state LEDs. Finally, the sixteen buffered input stages can be connected to a PC via a parallel port or other 8bit TTL data input (plus control output), allowing the Logic Visualiser to actually function as a logic analyser with the aid of appropriate computer software.

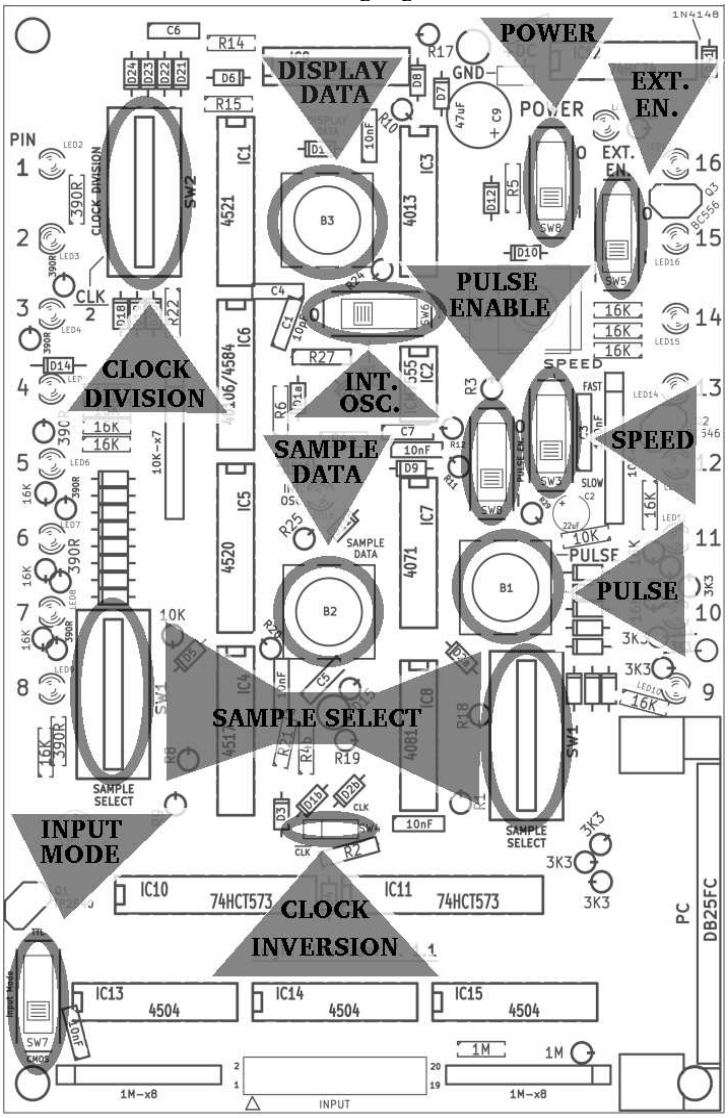
Inputs	16 + Clock, Trigger, & Vinput
Input Impedance	1Mohm
Max. Input Frequency	Greater than 1MHz
Input Logic Level	TTL/CMOS
Input Voltage Range	5V TTL, 3−18V CMOS
Sampled Data Storage	127 bits
Data Outputs	8
Output Logic Level	TTL
Supply Voltage	Regulated 5VDC
Supply Current	Less than 100mA
Board Dimensions	150x100mm (LxW)

Table 1, Specifications.

Chapter I

Usage

The Logic Visualiser can function in a number of different modes, selected by the various switches and buttons highlighted below.



To Begin:
Before getting into the specifics of operation, here are some observations common to all the operating modes detailed in this chapter:

- Ensure that regulated 5VDC is connected to the Power pins with the correct polarity.
- The Ground and External Voltage connections must be connected to the external circuit ground and supply voltage for correct operation.
- Connect the External Trigger input to Ground when not in use to prevent false triggering.
- Check that the "**EXT. EN.**" switch to enable external control by the parallel port is not on when using the Logic Visualiser independently.
- If you power the Logic Visualiser from the same supply as the circuit being examined, take care not to accidentally connect the GND probe to a low impedance voltage source because sparks might fly!
- Check that the "Input Mode" switch selects the correct logic threshold mode to match the outputs from the circuit being examined.
- Vertically mounted slide switches are turned on by moving them down (towards the front of the board).
- Circuits operating at frequencies towards 1MHz and above may generate noise on unconnected inputs sufficient to cause them to register as High. Users may wish to connect unused inputs to a convenient GND point if this is distracting.

Mode 1: Internal Oscillator
Switch the "**INT. OSC.**" switch **ON**, and select **division 1** (CLK/2) on the "**CLOCK DIVISION**" DIP switch (not required if the optional R17 modification described in Chapter II has been performed) to enable Internal Oscillator sampling mode. In this mode a Clock input is not required and its probe can be left disconnected. Low frequency clock signals are generated according to the setting of the "**Speed**" switch and allow the current state of the inputs to be immediately observed ("FAST" setting), or to be occasionally sampled and displayed for up to a few seconds ("SLOW" setting). The latter mode is useful for fast changing signals where the pace of the busy inputs is too quick for the eye to see.

The potentiometer above the "Speed" switch allows the adjustment of the internal oscillator frequency with a little more finesse. Rotating this clockwise increases the frequency, and it is recommended that the furthest rotation in this direction be used as the default for the "FAST" speed

selection, to ensure accurate display. By carefully adjusting the potentiometer in the "FAST" range, it is possible, for input signals operating at frequencies up to the lower KHz, to find a division of this frequency that makes repeating input changes directly visible. To aid this, a logarithmic potentiometer is used, with the effect of expanding the lower frequency end of the adjustment range. Turn the knob while watching for a spot where the display pauses or flickers more slowly, then very slowly scan around this point until you find a position where the display begins to advance visibly in sequence.

The LED at the center of the the board shows the clock signal generated by the Internal Oscillator.

Mode 2: Pulse
The configuration here is the same as for Internal Oscillator mode, but with the "**PULSE EN.**" switch, to the left of the speed selection switch, **ON**. Now you are awarded direct control over the sampling, provided in the form of the "**PULSE"** button. Each press toggles between the sample and display states, so individual input states can be viewed for as long as required. The Internal Oscillator LED will flash to announce each pulse.

Performance in this mode when used with high frequency inputs may be improved when the internal oscillator speed is set to "FAST".

Mode 3: Clock Division
When the "**INT. OSC.**" switch is **OFF**, the clock input is taken from the Clock probe connected at the input, which may be inverted with the "**CLOCK INVERSION**" switch. This mode is controlled by the DIP switch at the top left of the board, marked "**CLOCK DIVISION**". The selection here determines the number of clock cycles after which the input states are automatically sampled. One clock signal is skipped from the count on each cycle so that the input will be sampled one clock period ahead of its relative position before. For repeating signals, this allows the input states to be shown in exact sequence.

Switch 1 of the Clock Division selection does not perform the above behaviour, instead sampling the inputs at half the frequency of the Clock input. For input clock frequencies faster than can be seen with the eye, this will provide a similar display to the Internal Oscillator "FAST" mode, with the input states effectively shown in "real–time". The higher switch selections sample at far greater divisions of the clock frequency, allowing fastly clocked input states to be examined individually. With no division selection made, the input display is paused in its last state.

Switch	Division
1	2
2	262,144
3	524,288
4	1,048,576
5	2,097,152
6	4,194,304
7	8,338,608
8	16,777,216

Table 2, CLOCK DIVISION settings.

The "**CLOCK INVERSION**" switch should be changed depending on whether the input signals are rising or falling edge clocked. Note that the opposite setting should be used in Data Sampling mode.

Mode 4: Data Sampling

When an external clock signal is applied to the Clock input, 127 bits of data can be serially sampled from any one of the sixteen data inputs. The input to be sampled is selected on one of the two "**SAMPLE SELECT**" DIP switches at either side of the board. These are orientated relative to the input state LEDs, so that switch 1 of the leftward DIP switch selects input 1, while switch 1 of the rightward DIP switch selects input 9, and switch 8 on the same DIP switch selects input 16. Only one input selection should be active at a time.

With the pin of interest sorted out, pressing the "**SAMPLE DATA**" button records 127 bits of the input data to memory, during which time the input state LEDs are blanked (at high clock frequencies this may not be visible). With this complete, the data may be displayed by pressing the "**DISPLAY DATA**" button while "**INT. OSC.**" is **ON**, and the "**SPEED**" switch is in the "**SLOW**" position. Beginning at the input 1 LED, data is then shown scrolling down the left row of LEDs and up the right, the previously displayed input state being pushed off ahead of it.

An alternative method for triggering the sampling is to let a signal take the driver's seat by connecting it to the "**EXT. TRIG.**" input. This allows an electronic signal in the external circuit to cause the input cycle to begin. For capturing intermittent bursts of data less than 128 bits in length, it can even be connected to the same signal as the selected data input, because once begun, further pulses will not restart the sampling until it has reached the end of memory. Note that when using this sampling method the data display should be fully advanced to the end, otherwise the order of the new data will be mixed up. Also the sample input mode should not be triggered during

data display or some very confusingly corrupted data will be the result.

The controls for the Internal Oscillator and Pulse modes vary the rate of the data as it scrolls across the display. The potentiometer varies the speed, while selecting the Pulse control allows the display to be manually advanced. Pressing "DISPLAY DATA" again returns to the input state display, with the sequence resuming from the position at which it was left if the button is pressed again before new data is sampled. Briefly switching the internal oscillator mode to "FAST" while in data display mode easily skips to the end of the data sequence, whereafter it can be viewed again from the beginning by another press of "DISPLAY DATA" after the speed has been set back to "SLOW".

The "**CLOCK INVERSION**" switch should be in the opposite position to that normally required for Clock Division mode. Incorrect setting will likely lead to corrupted data.

Mode 5: External Output
For use with a computer via parallel port or other interface, the "**EXT. EN.**" switch is moved downwards to the **ON** position. The device is now controlled by the signal at pin one of the DB25 connector, and multiplexes data on the following eight pins according to its state. The computer must toggle the multiplexer input signal in order to update the output data. The settings of other configuration switches in unimportant, though the "SHIFT IN" and "SHIFT OUT" buttons are best left alone.

Mode 5a: Alternative External Output (modification required)
With the relevant modifications described in *Chapter III* applied, the Logic Visualiser can be used by software not designed for the multiplexed output method used by the normal external output mode.

Connect the dedicated input cable described in *Chapter III*, then set the "**SAMPLE SELECT**" switches with all even switches of the leftward DIP switch **ON**, and all odd switches of the rightward DIP switch **ON** also. The active switches on the left should therefore be:
2, 4, 6, 8
and on the right:
1, 3, 5, 7

Finally, install the three jumpers on the board and configure the switches for "Pulse" mode, press the "pulse" button once if the LEDs are off then leave it to its own devices.

Chapter II

Construction

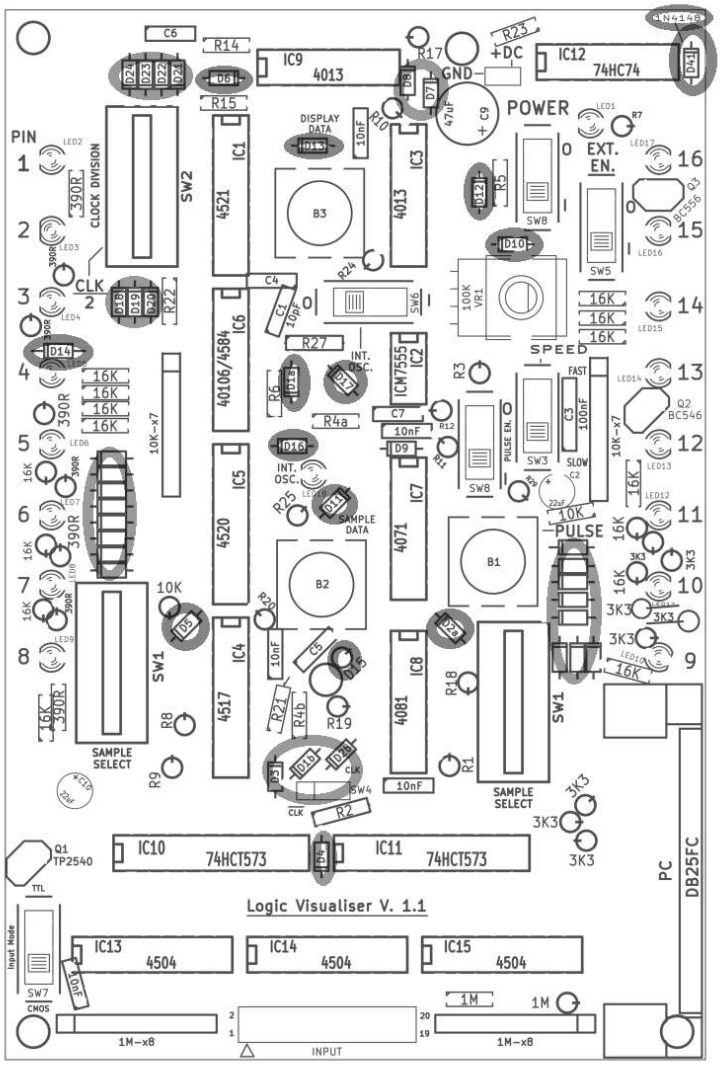
If you are reading this as a printed booklet supplied with the Logic Visualiser kit from OmberTech, your surrounds should be awash with the many and varied components detailed in Table 3, as well as a lonely circuit board awaiting their acquaintance. This chapter describes a convenient sequence for the assembly of the board and its connecting test cable.

Note that there is a section describing optional modifications at the end of this chapter which is probably best considered before you begin construction.

Part	**QTY.**	**IDs**
LED	18	LED1–LED18
TP2540 P–Type FET	1	Q1
BC54x NPN Bipolar Transistor	1	Q2
BC55x PNP Bipolar Transistor	1	Q3
10pF Ceramic Capacitor	1	C1
22uF Electrolytic Capacitor	2	C2, C10
100nF MKT Capacitor	1	C3
100nF Ceramic Capacitor	1	C4
10nF MKT Capacitor	8	C5–C8, C11–C14
47uF Electrolytic Capacitor	1	C9
BAT86 Schottky Diode	42	D1a/b, D2a/b–D40
1N4148 Silicon Diode	1	D41
4521 24bit Counter IC	1	IC1
ICM7555 CMOS Timer IC	1	IC2
4013 Dual Flip Flop IC	2	IC3, IC9
4517 Dual 64bit Shift Register IC	1	IC4
4520 Dual 4bit Counter IC	1	IC5
40106 Hex Schmitt Inverter IC	1	IC6
4071 Quad OR Gate IC	1	IC7
4081 Quad AND Gate IC	1	IC8
74HCT573 Octal 3–State Latch	2	IC10, IC11
74HC74 Dual Flip Flop IC	1	IC12
4504 Hex Level Shifting Buffer IC	3	IC13–IC15
16 Pin DIP IC Socket	3	
8K2 Resistor	2	R1, R2
16K Resistor	27	Rxx, R3, R4a/b, R6, R14, R15, R17, R18, R20, R22, R23, R29
150K Resistor	3	R5, R21, R24
390R Resistor (383R in kit)	10	Rxx, R7, R25
10K Resistor	3	Rxx, R10
2K2 Resistor	2	R11, R12
3K3 Resistor	8	Rxx
1M Resistor	4	R16, R19, R26, R27
1Mx8 SIL Resistor Module	2	Rxx
10Kx7 SIL Resistor Module	2	Rxx

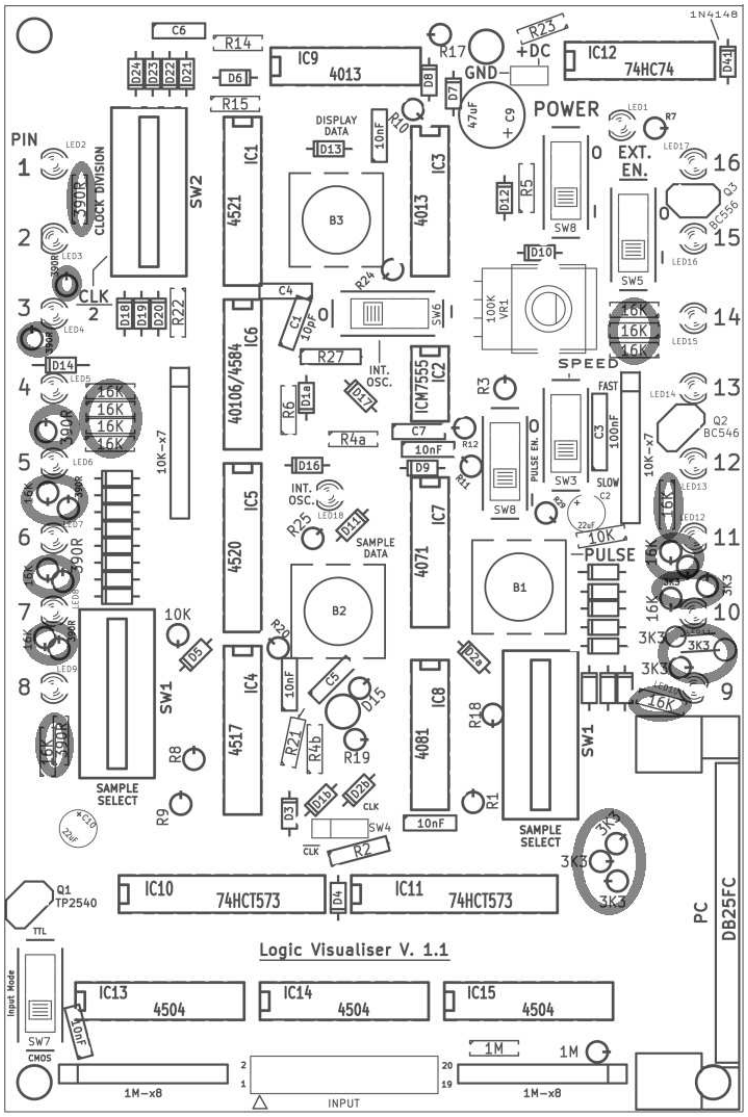
Part	QTY.	IDs
100K Log. Potentiometer	1	VR1
Potentiometer Knob	1	
8x DIP Switch	3	SW1(Red), SW2(Blue)
DPDT Slide Switch	6	SW3, SW5−SW9
SPDT Miniature Slide Switch	1	SW4
Tactile Switch	3	B1−B3
Tactile Switch Caps	3	
20 Pin Pin Header	1	INPUT
2 Pin Pin Header	1	POWER
20 Pin IDC Connector	1	
Ribbon Cable 20way x0.5m	1	

Table 3, Parts List. Note that resistors with ID "Rxx" are marked by value on the circuit board silkscreen. Extras are supplied in the kit for many of the more numerous component values.



Diodes – BAT86x42 (D1a/b, D2a/b – D40) 1N4148x1 (D41)

Install all the diodes ensuring that the end with the band indicating polarity matches the mark on the silkscreen. D15 should be inserted with the band facing the circular mark on the silkscreen. Take care to use the 1N4148 diode for D41 instead of just another BAT86. If using an external rotary switch for SW2, the diodes around the DIP switch outline can be omitted, see *Optional Modifications* .



Perimeter Resistors: 390R (x8), 3K3 (x8), 16K (x15)

These resistors for the sixteen input/output stages were not awarded individual component IDs like those proudly worn by the other components on the silkscreen, but are all of the above three values. The 390R resistors are provided as 383R resistors in the kit, and are actually surplus 0.25% tolerance types – almost criminally wasted here for mere LED current limiting.

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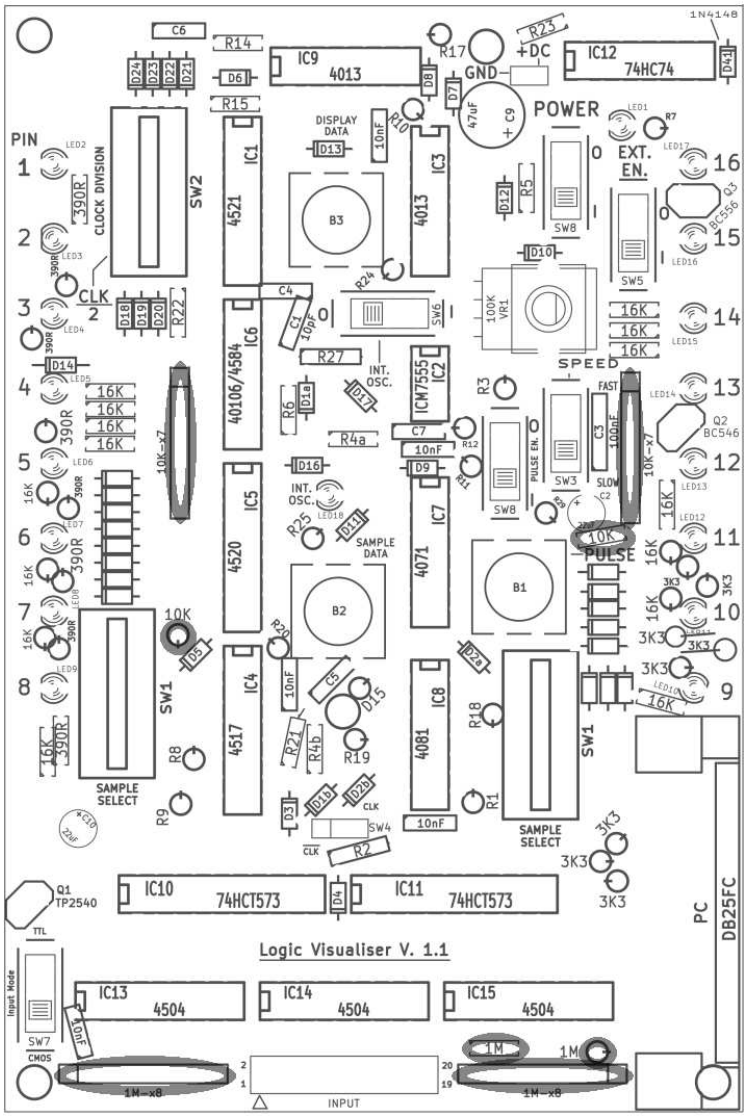
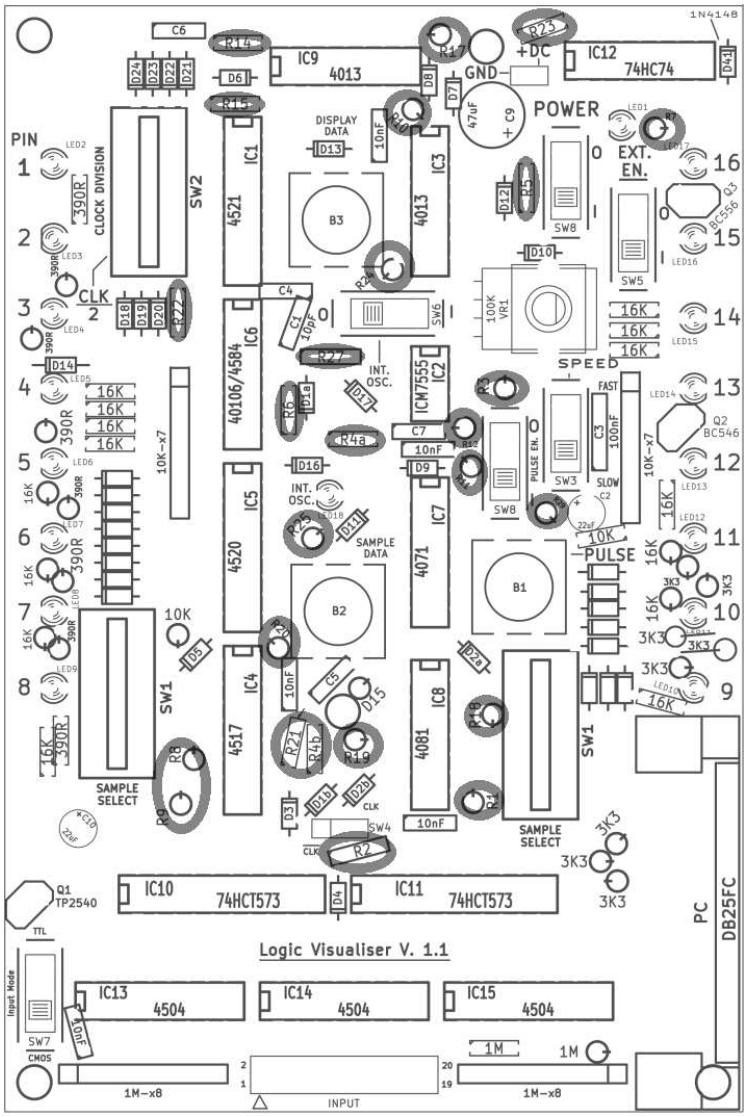


Resistor Modules: 10K–x7 (x2), 1M–x8 (x2), 10K (x2), 1M (x2)

Now the pull–down resistor modules are installed, along with some other lonely single resistors in association. Ensure that the common pin of the modules, indicated by the dot at one end, is correctly positioned at the boxed end of the silkscreen image.



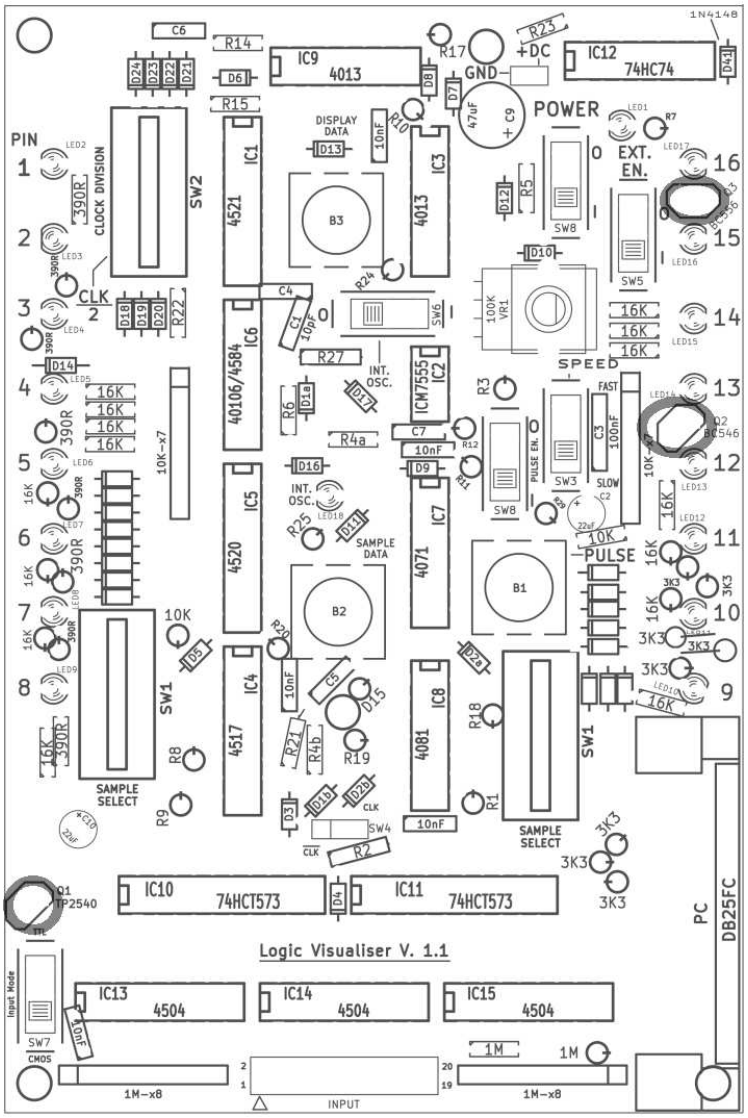
Internal Resistors: 390R (x2), 1K (x2), 2K2 (x2), 8K2 (x2), 10K (x3), 16K (x12), 150K (x3), 1M x2

Now the remaining resistors are installed, see the following table for values (the value–less resistors don't exist). 1K1 resistors are provided in the kit for the 1K positions. Note that there is an optional (but recommended) modification to R17 hiding in the *Optional Modifications* section at the end of this chapter.

Identifier	Value
R1–R2	8K2
R3	16K
R4a/b	16K
R5	150K
R6	16K
R7	390R
R8–R9	1K
R10	10K
R11–R12	2K2
R13	
R14–R15	16K
R16**	1M
R17*–R18	16K
R19*	1M
R20	16K
R21	150K
R22–R23	16K
R24	150K
R25	390R
R26**–R27	1M
R28	
R29	16K

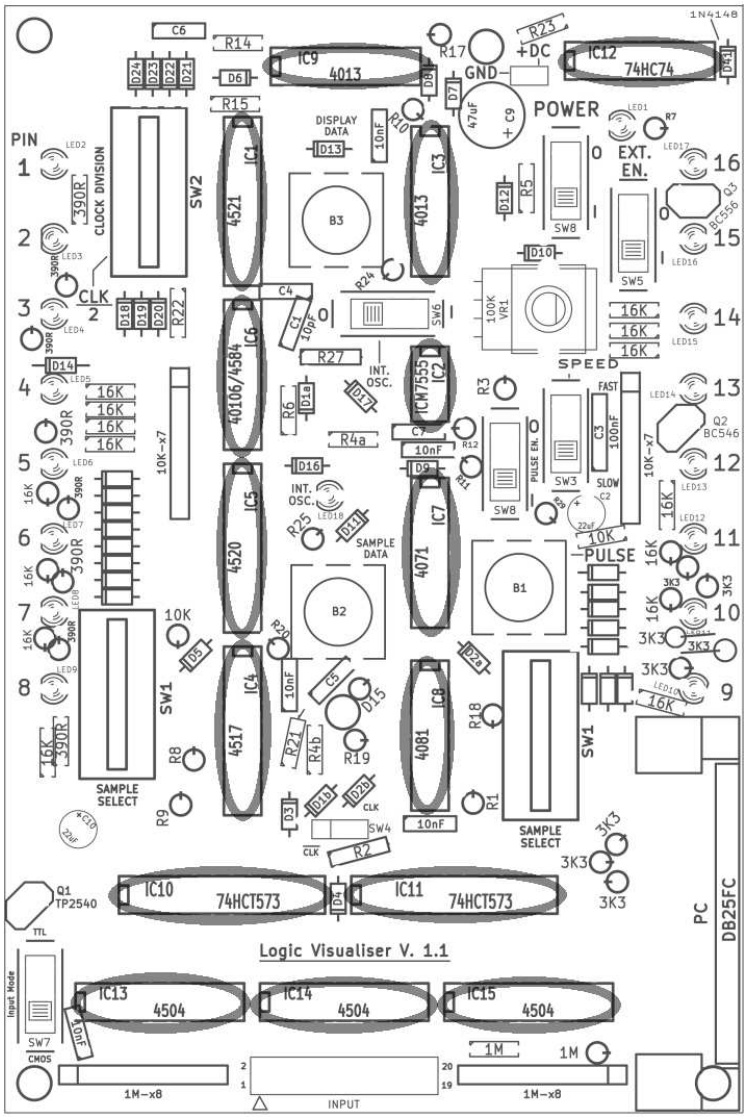
Value	Identifier
8K2	R1, R2
16K	R3, R4a/b, R6, R14, R15, R17*, R18, R20, R22, R23, R29
150K	R5, R21, R24
390R	R7, R25
1K	R8, R9
10K	R10
2K2	R11, R12
1M	R16**, R19*, R26**, R27
3K3	

Table 4, Resistor Designations, *Modification described in *Optional Modifications*.
**Included in Resistor Modules or Perimeter Resistors section.



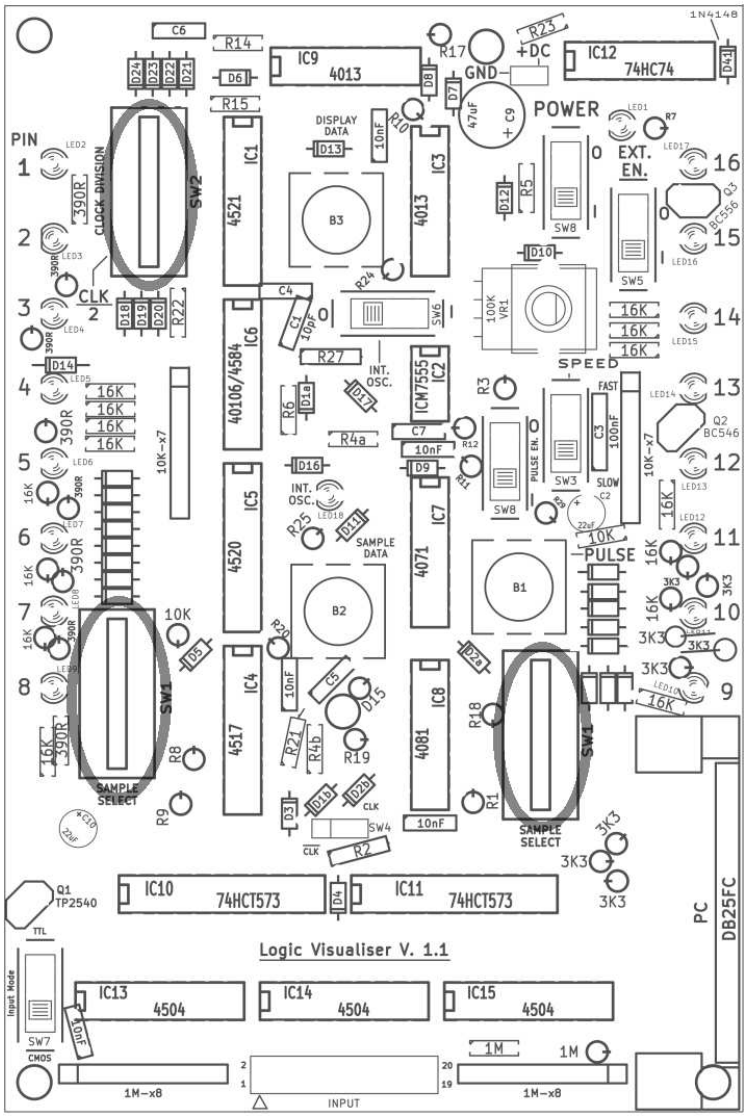
Transistors: BC549 (Q2), BC556 (Q3), TP2540 (Q1)

Now for the transistors. Make sure that the orientation matches the silkscreen image. Note that Q1 (TP2540) is a FET so precautions should be taken to prevent static discharge. At a minimum, touch the metal case of a grounded piece of equipment on your bench before handling the FET. Ignore the fact that Q2 is marked BC546 on the silkscreen, actually the circuit isn't picky about any breed of BC54x or BC55x transistor used.



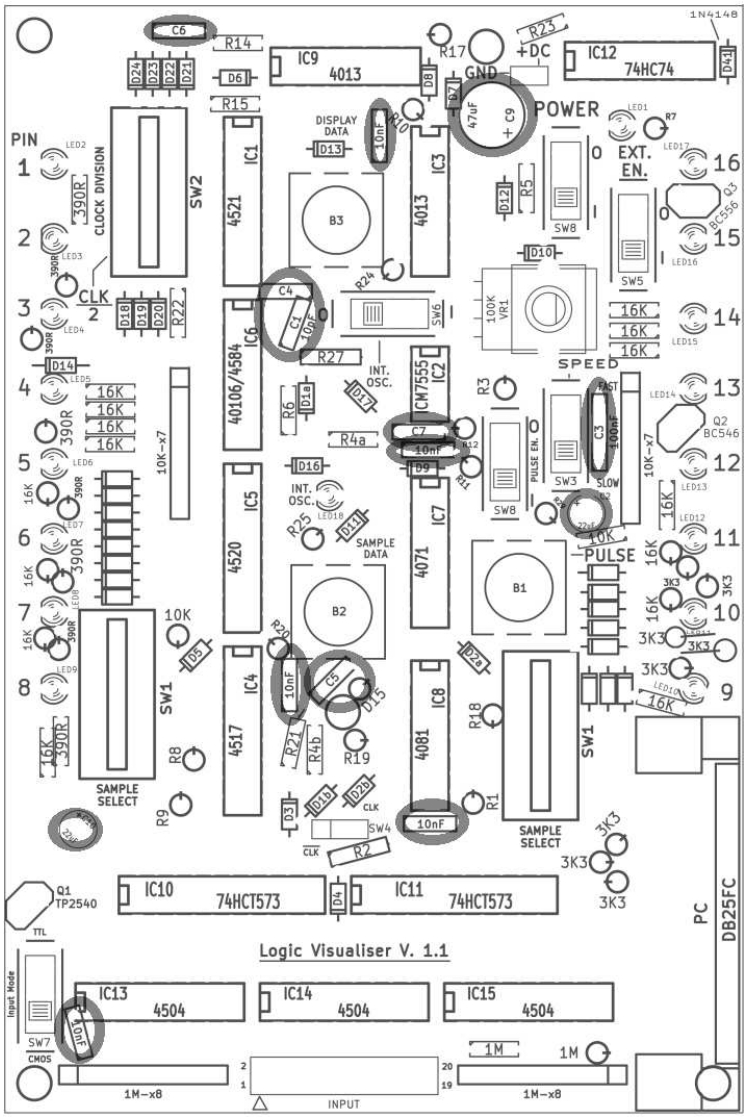
Integrated Circuits: IC1–IC15

Now the big moment, the integrated circuits are installed. Note that these also have a (lesser) chance of damage by static discharge, and again take care that the orientation matches the silkscreen. Remember to install sockets for IC13–IC15 at the bottom, no need to install the 4504 ICs in these yet. Although not provided for in the kit, there's no reason that all the ICs couldn't be socketed, if that's more to your taste.



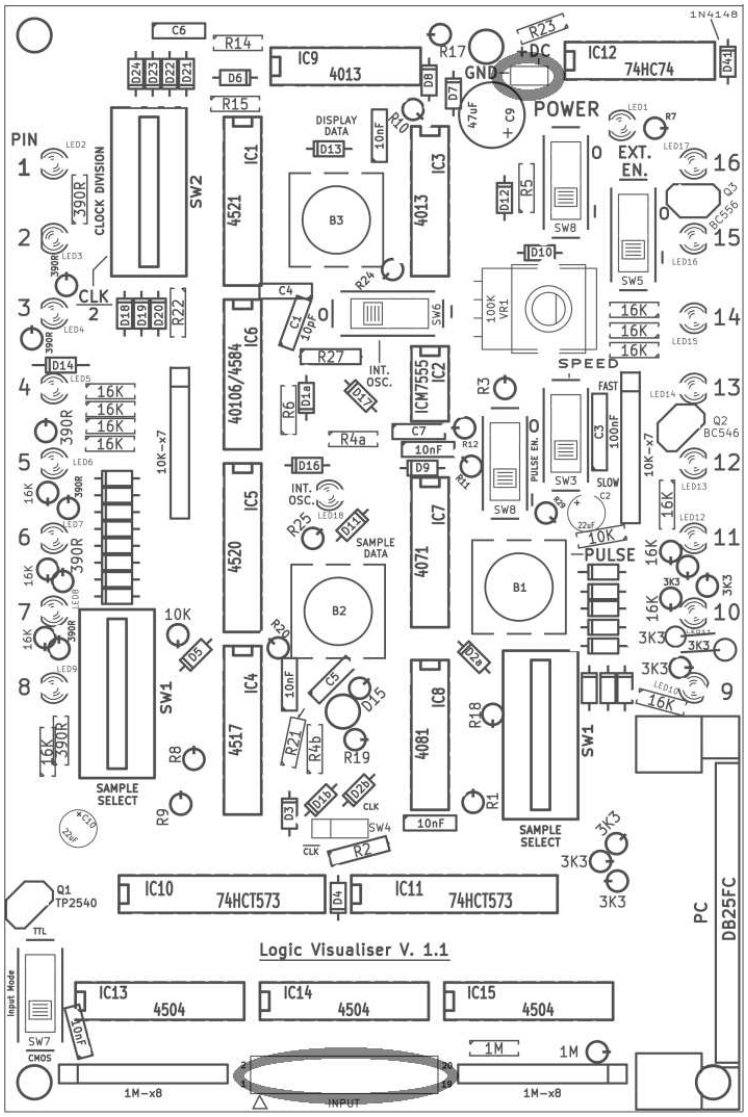
DIP Switches: SW1, SW2

Now for the DIP switches that select the data sampling input and the clock division factor. Check the orientation, with switch 1 at the square pad. If DIP switches aren't good enough for you, see the *Optional Modifications* section for how to use external rotary switches instead.



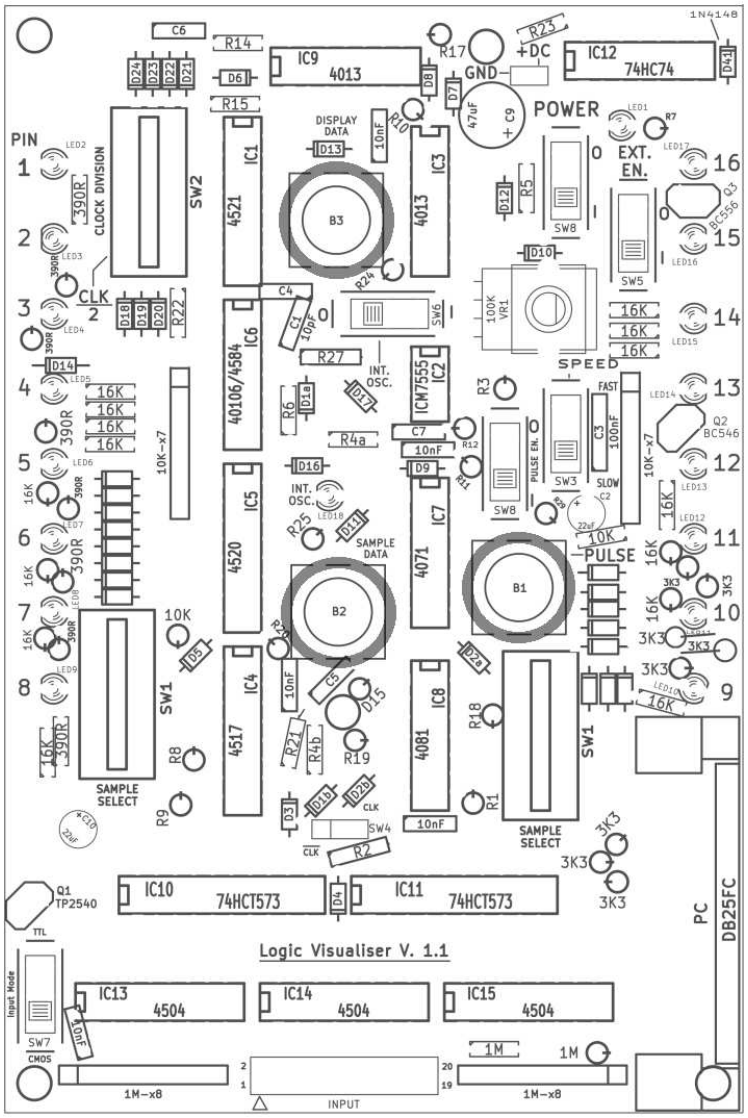
Capacitors: 10pF (C1), 10nF (C5–C8, C11–C14), 100nF (C3, C4), 22uF (C2, C10), 47uF (C9)

Install the capacitors as shown. The electrolytic capacitors can be bent over to keep them below the LED height. 10nF filter caps above C7 are only labeled by value on the silkscreen.



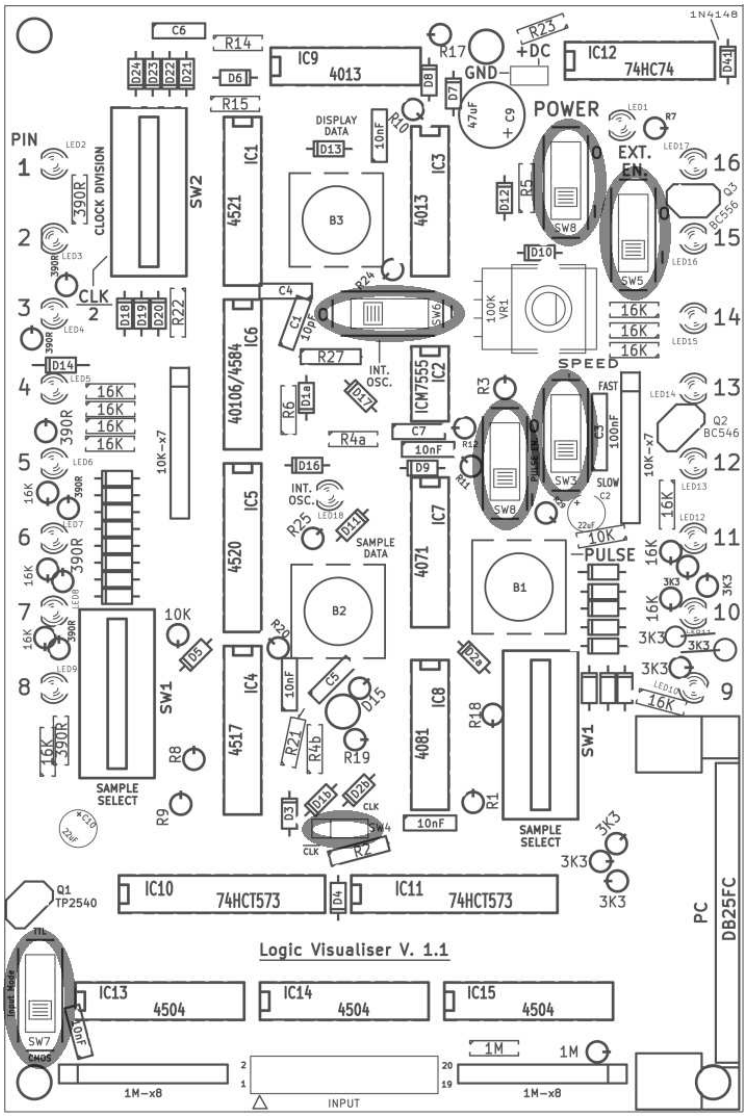
Input Connector and Power Pins:

The input connector should be positioned with the alignment notch towards the edge of the board, so that pin one is located as indicated by the triangle on the silkscreen image. The power pins can be installed as well, if used.



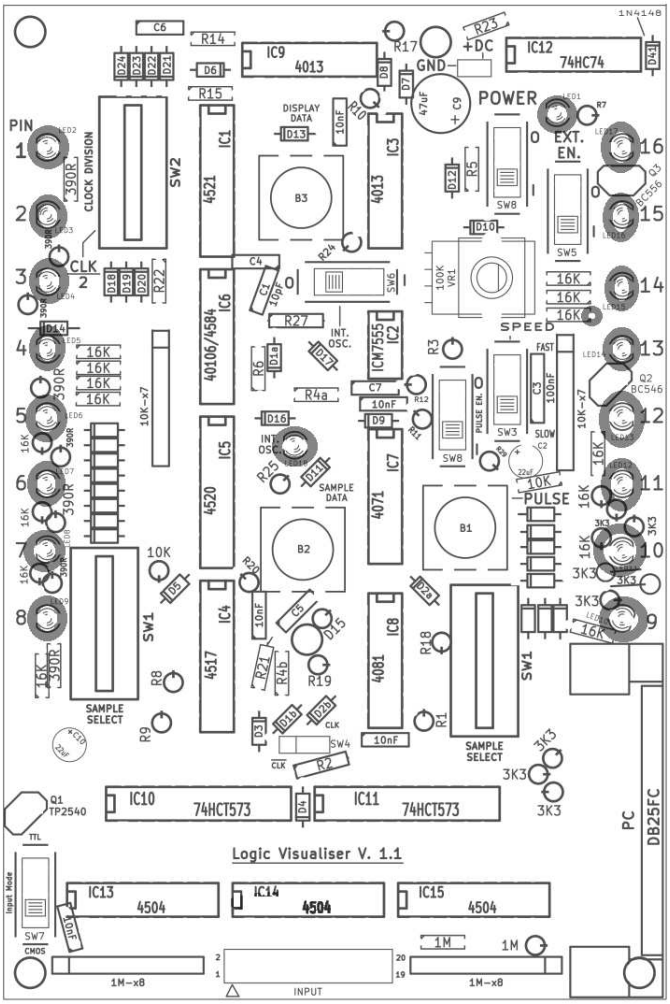
Buttons: B1–B3

Now for the buttons. These press in to position before soldering, orientation is not important.



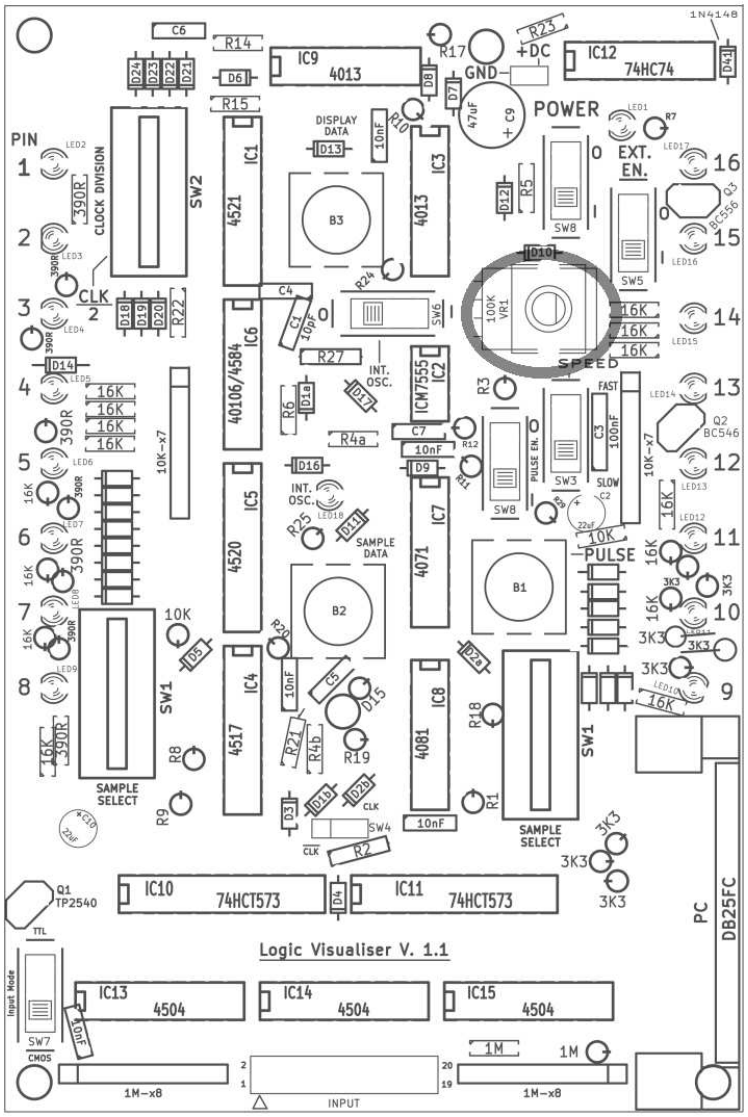
Switches: SW3, SW5–SW9

The switches are now installed. Make sure to solder all the mount points around body of the switches as some are sneakily used as ground connections for parts of the circuit. Things are a bit tight around SW4, so it might end up a little crooked. POWER switch SW9 is pretending to be SW8 on the PCB V. 1.1 silkscreen, though they're both the same type anyway.



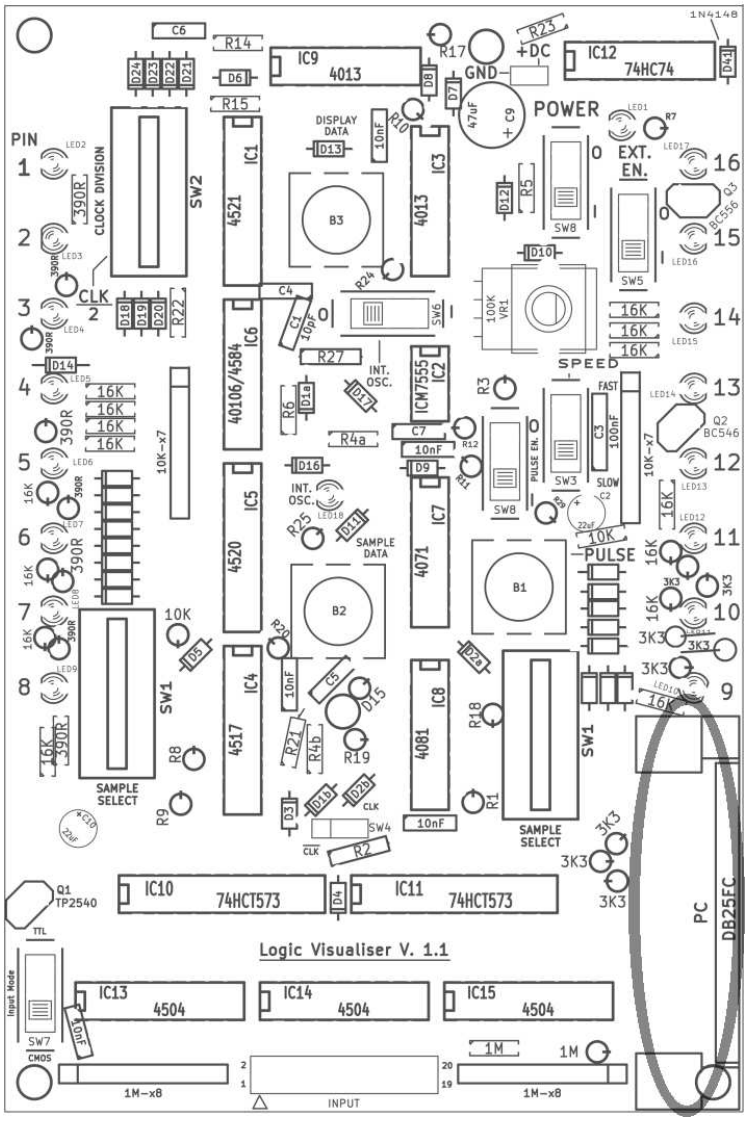
LEDs: LED1–LED18

The LEDs around the perimeter, as well as the Power and oscillator LEDs, are now soldered. These should be installed at a height sufficient to stand above the top of the other components and through the case above. The leads of the LEDs have lumps that can be used to set the height above the board. Watch that the notches on the sides match the silkscreen. Unfortunately the anode of LED14 (input 13) was left unconnected on board V. 1.1, so solder its lead to the pad of the closest 16K resistor, as shown circled, before trimming it off.



Potentiometer: VR1

The 100K Logarithmic potentiometer is now pressed into place and its pins and mounting lugs soldered to the board.



Parallel Port Connector:

If used, the 25 pin D−type socket for connecting to a PC for use with the logic analyser software can be soldered in place. The mounting holes are a little bit out of position for the connector supplied with the kit, so the mounting lugs have to be bent towards the board edge slightly in order to fit into position.

Final:

Construction of the Logic Visualiser circuit board is now complete. The caps for the buttons can now be pressed on to the square mounting lugs. The 4504 ICs (IC13–IC15) that you thought I'd forgotten about can finally be inserted into their sockets, and also the knob for the potentiometer can be installed, with the grub screw tightened onto the flat section of the potentiometer shaft. Note that the knob will need to be removed later if a case is to be installed over the top of the circuit board.

Accessories:

The cable for the inputs to the Logic Visualiser can now be assembled using the included IDC socket and ribbon cable, as well as the separately purchased test probes/clip/etc.

The IDC socket is first assembled on the end of the cable by pressing the top section down using large pliers or even a small hammer, while the the cable is sandwiched between it and the body of the connector. If the cable is already marked for pin 1, be sure that this side enters the connector at the end indicated by the small arrow. The cable should be inserted so that it flows *inward* to the circuit board when the socket in plugged in.

Once the socket is installed on the cable, the cable can be pulled back over the top of the socket as the retaining bar is pressed down on top of it, so that the cable now flows away from the Logic Visualiser circuit board.

The test connectors chosen to be used by the constructor may now be attached to the other end of the cable. The method for this will vary depending on the type of connector used, but the following table describes the associations of the wires in the order they are presented at the cable (sorry, no there isn't logic in there somewhere).

Wire No.	Function
1	External Trigger
2	Signal Ground (GND)
3	Input Pin 5
4	Input Pin 3
5	Input Pin 4
6	Input Pin 1
7	Input Pin 6
8	Input Pin 2
9	Input Pin 8
10	Input Pin 16
11	Input Pin 7
12	Input Pin 15
13	Input Pin 9
14	Input Pin 14
15	Input Pin 10
16	Input Pin 13
17	Input Pin 11
18	Input Pin 12
19	Clock Input
20	External Supply Voltage Input

Table 5, Test Cable Wire Functions.

Optional Modifications

R17 Internal Oscillator Override Modification:
Normal operation of the Logic Visualiser requires that the first switch of the "Clock Division" DIP switch be selected in order for the internal oscillator mode to function. This modification allows the internal oscillator mode to automatically function regardless of the clock division setting.

The modification involves connecting R17 to pin 4 (RST) of the oscillator IC2, instead of pin 13 (Q) of IC3b. To do this, leave the standard position of R17 unpopulated and instead wire it on the under side of the board between pin 8 of IC9 and the lower (closest to the input connector) middle pin of SW6. The resistor leads may need to be covered to prevent them from shorting against other solder joints.

Alternative External Output Modification:
This modification allows the Logic Visualiser's external outputs to be used with software and devices that don't have the courtesy to output the multiplexing signals that the normal external output mode requires in order

to update the outputs. As such it offers only eight outputs instead of the normal multiplexed sixteen.

This modification requires one 200ohm (or 180ohm) resistor and three jumpers to be added to the board, as well as a dedicated test cable to be built that connects the unused inputs to GND.

The new resistor is connected in parallel with R19 which connects between pin 2 of IC8 (input from SW1) and GND, but with the jumper (J1) connections interrupting the circuit when no jumper is installed. The other jumpers connect pin 11 of IC10 (J2) and IC11 (J3) to Vcc (pin 20 of the same ICs). Use wire to connect between the jumper terminals and the board, then glue the terminals in a convenient location on the board.

The dedicated input cable is constructed as usual except for the pins specified in Table 6 as being connected directly to GND (corresponding with the eight unused inputs). If the cable will be used for no other purpose, the Clock Input (**19**) and External Trigger (**1**) pin connections could be omitted and also connected to GND.

It is essential that the dedicated test cable be connected whenever the jumper associated with R19 (J1) is inserted, otherwise damage may result. Best practice is to connect J1 to the dedicated test cable and make excess cable available at the input connector while the jumper cable is taut. This makes it difficult to remove the input connector without first disconnecting the jumper.

Wire No.	Function
1	External Trigger (Not Required)
2	Signal Ground (GND)
3	Input Pin 5
4	Input Pin 3
5	GND
6	Input Pin 1
7	GND
8	GND
9	GND
10	Input Pin 8
11	Input Pin 7
12	GND
13	GND
14	Input Pin 6
15	Input Pin 2
16	GND
17	GND
18	Input Pin 4
19	Clock Input (Not Required)
20	External Supply Voltage Input

Table 6, Alternative External Output Test Probe Cable Pinout.

External Switches:
For easier use, or general bling, the Logic Visualiser could be built with the full luxury of externally mounted rotary switches in place of the SW1 and SW2 DIP switches. Simply connect the common rows of the DIP switch pins to the center poles of the rotary switches. if a rotary switch with "break before make" type contacts is used for SW2, the seven series diodes can be replaced with one single diode in series with the switch pole, with its anode towards IC9b's clock input. These diodes are only only included on each switch to protect IC1's outputs from being shorted against each other if multiple selections are accidentally made on the DIP switch.

Initial Checks

With the full mess of componentry now consolidated into one almost hand–held lump of electronic wizardry, it is tempting to now power up and be bedazzled by the many lights of logical insight that you have toiled to install. But first you must be sure that no small error could cost you all your work, and even the components that this whole creation relies on.

Begin by checking visually for missed or bridged solder joints, touching component leads, and any components that have mysteriously turned themselves around to face the wrong way since you carefully orientated and soldered them during construction – such mischief can have consequences for ICs, Transistors, Diodes, LEDs, Electrolytic Capacitors, and the SIL Resistor Modules. With these faults now either fixed or unobserved, it's time to bring out the electronic eye of your multimeter and scan it for any faults that your own eye failed to observe. In resistance mode, check there is no short between Vcc and GND. Next you might also want to check between the adjacent pins of all the ICs in case there is an unseen bridge between them, but this will be a slow process so whether it is required depends on the confidence you hold in your own visual examination.

Now it's finally time to skip back to that alluring chapter about "usage" that you were glancing enviously at earlier, and excite yourself terribly over the many and varied functions awarded to you by the componentry that you have so carefully assembled. Good luck!

Chapter III

Circuit Description

Part 1: Schematic
The full schematic is too large to include here, so it is supplied separately in the kit and should be referred to throughout this chapter. Only the first three input stages are shown, with the others following the same pattern. The LE and #OE inputs of each IC10–IC11 latch are connected together internally, and are not connected between the two ICs.

Note that D1, D2 and R4 are duplicated for the #OE input to IC11. These are shown on the PCB as D1a/b, D2a/b and R4a/b. R4b connects with SW5b, while the diodes connect with the same signals as their "a grade" counterparts.

For connections with the external outputs, and the full output LED circuit configuration, a separate diagram is shown in Part 3.

Part 2: Circuit Overview
At intervals determined by the circuitry associated with the active operating mode, the IC10–IC11 (74HCT573) 8bit Latching Bus Buffers alternate between sampling input data and displaying it on the sixteen output LEDs. In the Internal Oscillator and Pulse operating modes this sampling occurs at an interval determined by the user, whose wishes are converted into electronic commands by IC2 (ICM7555), a CMOS version of that ever popular NE555 timer IC which does so love to pop up in circuits like this.

A slightly more involved sequence of interactions is required for the Clock Division mode which must ensure that the input is sampled one clock period after the relative position where it was sampled previously, and at slow enough intervals that the human operator is still kept in on the fun. The IC1 (4521) 24 Stage Counter IC with its seven output taps provides a suitable delay between updates. Meanwhile dual flip/flop IC9 (4013) triggers the input latches at the end of a cycle, while simultaneously preventing IC1 from seeing the following clock pulse, so that its count will inadvertently "gain" one ahead of its last cycle.

In External Output mode, the timing signals are left entirely to the judgment of whatever computer, or other device, chooses to talk on the LPT SELECT input. Whether this input is High or Low determines whether the first or second bank of eight latches (IC10–IC11) is showing its latched data on the data outputs.

Things are a little different for Data Sampling mode. For data input, all the data latch outputs are disabled and the input is taken straight from the input buffer selected by SW1. A signal on the External Trigger input, or a user pressing the Sample Data button, causes the data to be shifted into IC4 (4517) Dual 64bit Shift Register while IC5 (4520) Dual 4bit Binary Counter waits until it's full. IC3 (4013) Dual Flip/Flop starts this sequence when the B2 push button or External Trigger input is asserted, and when the IC5 counter reaches 128, it is reset and the device gets back to what it was doing before.

Data display operates similarly, except that now the IC13–IC15 (4504) input buffers are disabled instead of the latches, and the latch outputs are constantly enabled so that IC10–IC11 acts as one big parallel output shift register. Data is fed into this from IC4, while the same data is fed back to its own input so that it can be viewed again later. Again, the IC5 counter stops the sequence when the end of the stored data is reached by resetting IC3 which began the display by latching the input from B3.

In the optional Alternative External Output mode, the input latches are configured in "transparent" mode, where they act simply as further data buffers. Alternate inputs to IC10–IC11 must be pulled low to prevent data "flowing through" between inputs and outputs as in Data Sampling mode during display.

Full Circuit Description

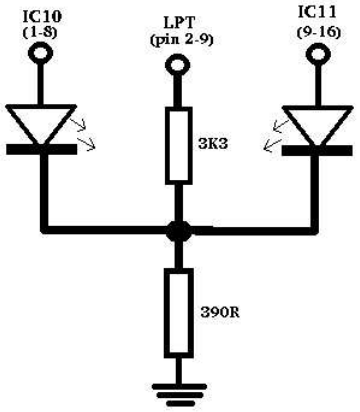
Part 3: Input/Output

The Logic Visualiser circuit is is designed to work in any of five operating modes described in Chapter I: **Internal Oscillator, Pulse, Clock Division, Data Sampling,** and **External Output**. At the circuit level, the common factor unifying these many any varied processes is the input/output sections of the circuit consisting of IC10–IC11 8bit Latching Bus Buffers, and IC13–IC15 Level Converters. The influence of the Data Sampling mode weighs heavily on circuit design between the IC13–IC15 (4504) outputs and the IC10–IC11 (74HCT573) inputs. The 4504 does not have 3–state outputs, but due to its unusual input design, when the supply voltage is disconnected from its Vdd pin, it will not source any current at its outputs even when an input is High. With the series diode, the outputs can therefore be effectively disabled by switching off the supply voltage, this is achieved with FET Q1 (TP2540) which has a suitably low on resistance.

Between the outputs of the data latches and the following inputs, 16K resistors allow data to be fed forward through the latches in Data Sampling output mode so that they act as a Serial–In Parallel–Out (SIPO) Shift Register. With the diodes on the outputs of IC13–IC15 preventing them from sinking current, pull–down resistors are also required on the data latch

inputs. 10K resistors are used for this purpose, but they can not be directly connected to GND as this would prevent the 16K resistors used in the "shift register" configuration from pulling the latch inputs sufficiently High. To solve this, Q2 (BC54x) turns off the GND connection to the pull down resistors when the #SHIFT OUT signal goes Low, indicating Data Sampling output mode. However things still aren't right because this leaves all the data latches connected together via 10K resistors and a common voltage may rise high enough to force them all High. This is countered by the odd−looking inclusion of D41 (1N4148) in parallel with Q2. The approximate 0.7V forward voltage of this silicon diode is more consistent than the schottky BAT86 diodes used elsewhere, and is used to prevent the voltage rising too high, while setting a high enough minimum voltage that the High inputs from the previous stage are not pulled below the TTL High threshold of the IC10−IC11 inputs.

The output circuit is not completely shown in the full schematic. The below diagram shows how the outputs of IC10 and IC11 are connected via the logic state LEDs to the external output through a 3K3 resistor (note that the 16K feed−forward resistors are not shown):



The 3K3 resistors protect against misconfigured software setting the data pins as outputs when the Logic Visualiser is connected to a bidirectional bus such as the suggested PC Parallel Port.

Part 4: Latch Control

In all operating modes except External Output, the Latch Enable (LE) inputs of IC10−IC11 are controlled by the IC12 (74HC74) Dual Flip−Flop IC. This is arranged in an odd configuration that causes the second Flip−Flop to reset the first as soon as it is clocked High. When IC12a is clocked by a Low to High transition on its Clock input, its #Q output goes Low causing the IC12b #SET input to be asserted which makes its #Q output go Low and asserts the #RST input to IC12a, resetting it's Q output that controls the LE

pins back Low. In doing so, IC12a's #Q makes a Low to High transition that clocks IC12b low again also, ready for the next cycle to begin. The purpose of this little dance is to generate a pulse to the IC10–IC11 LE input that is short enough that in Sample Data display mode only one advancement of the shift register style display is made with each clock pulse. This requires that the pulse be short enough that there is no time for the data to propagate beyond one latch, but long enough to meet the minimum pulse width required for the LE inputs. Because the latches are 74HCT series devices, a 74HC device, capable of similar speeds, is required to achieve the task.

The #OE pins of IC10–IC11 are pulled low by R4a/b whenever the "EXT. EN." switch is off. They are brought High via D1a/b and D2a/b to disable the outputs before data is sampled from the input buffers. This prevents data feeding forward via the 16K resistors (except in Data Sampling output mode where this is desired).

Part 5: Internal Oscillator

The internal oscillator is based on a common CMOS derivative of the NE555 timer IC, IC2 (ICM7555). The key cause for using a CMOS type is the reduced current required to reset the device at pin 4, allowing it to be directly connected to IC3b (4013). The oscillator functions in the conventional way with the timing capacitor connected at pins 2 and 6 being alternately charged and discharged between 1/3 and 2/3 of the supply voltage, as measured internally by the IC, while the output clock signal changes in sync. D10 allows a faster charge time for the timing capacitor than it takes to discharge through the 100K potentiometer, leading to a short High pulse being output (except when the potentiometer is at maximum clockwise rotation).

The internal oscillator is used in three operating modes depending on the SW3 (SPEED) and SW8 (PULSE) positions. Switching the SW3 speed setting determines whether or not C3 is connected in series with C2. When it is, the effective capacitance is reduced to a little under the value of C3, setting the speed to Fast.

In Pulse mode, the circuit is changed by SW8a/b to act as a debounce function for the B1 push button. Both ends of the timing capacitor/s are brought to Vcc by R11 and R12, until B1 is pressed causing a High to Low transition to be passed to the pin 6/pin 2 inputs of IC2 via the timing capacitor/s. The capacitor/s must then recharge before the oscillator output returns Low and a second pulse can be generated.

SW6a enables the internal oscillator by disabling the reset at pin 4 by bringing it High. In the modified circuit, this also makes the SET input of IC9b (4013) High, which forces the RST input of IC9a Low and ensures that

every clock pulse causes it to alternate between data sampling and data display mode.

Part 6: Clock Division
SW6b feeds the buffered external clock signal selected at SW4 to the Clock input of IC1 (4521) which is a 24 stage counter with outputs on its last seven stages. The output selected by SW2 transitions from Low to High after the count shown in Table 7. This clocks IC9b (4013), causing it to change state and for its #Q output to go Low, disabling IC9a's reset and allowing its output to go High on the next Low to High transition of the external clock signal. This disables the IC10–IC11 latch outputs via D2 and holds the OR gate on the IC1 clock input High so that it does not see the following clock transition. The wired AND gate consisting of D7, D8, and R10 at the IC12a input clocks IC12 from the inverted external clock signal while the IC9a Q output is High, which in turn causes the Latch Enable input of IC10–IC11 to be pulsed High and the input data to be sampled. When the next external clock pulse comes along, IC9a changes state again, so its Q output goes Low, enabling the IC10–IC11 latch outputs while preventing clock pulses from entering IC12a. Meanwhile its #Q output makes a Low to High transition, clocking IC9b via D6 so that it reasserts the IC9a Reset input and then everything stays in that state until IC1 gets around to the next Low to High transition on its selected output.

Switch	Output	Division
SW2a	N/A	2
SW2b	Q18	262,144
SW2c	Q19	524,288
SW2d	Q20	1,048,576
SW2e	Q21	2,097,152
SW2f	Q22	4,194,304
SW2g	Q23	8,338,608
SW2h	Q24	16,777,216

Table 7, Clock Division Settings.

If the first switch of SW2 is selected (SW2a, "CLK/2"), the Set input of IC9b is forced High, bringing the Reset input of IC9a permanently Low so that the external inputs are sampled on every second external clock pulse. The series diodes on the IC1 outputs protect them from shorting against each other if multiple DIP switches are accidentally left on at once, while also forming part of an AND gate with D6 and R15.

Part 7: Data Sampling Input
The data sampling input mode can be triggered by either an external signal at the External Trigger input, or by the depression of push button B2. In either case this clocks flip/flop IC3a (4013) which causes its Q output to go

High because its Data input is connected to Vcc. If B2 is the source of the clock pulse, C5 also passes a High pulse to the Reset pins of counter IC5 (4520), via D15. This makes sure that the counter is reset in case data sampled previously was not fully displayed before the display sequence was canceled. This is not done for the External Trigger input because it would introduce a delay before acquisition began, and also in case it is desired to connect this to the same signal as the data input and record a sequence shorter than 128 bits as soon as it begins. If the counter were reset each time External Trigger went High, the data before the last bit would be wiped.

With the Q output of IC3a (labeled SHIFT IN on the schematic) High, the output of the IC10–IC11 latches is turned off via D1a/b on their #OE inputs. This prevents the feed forward resistors influencing the input data and indicates to the user that the data sampling sequence is in operation. The SHIFT IN signal also enables the clock signal to flow through IC8c from which it passes through IC7c to the clock inputs of Dual 64bit Shift Register IC4 (4517) and Dual 4bit Binary Counter IC5 (4520). While #SHIFT OUT is Low, the logic network at the data input to IC4 provides data from the input selected by SW1. This data is clocked into IC4 by the external clock signal until IC5 reaches a count of 128, whereafter it resets IC3, as well as itself, via D16, terminating the data input sequence.

Part 8: Data Sampling Output

The clock input of flip/flop IC3b (4013) from B3 requires debouncing because it toggles on each press to allow pausing the display sequence. This is provided by C4 which must recharge between each input pulse. A schmitt inverter is required to "square up" the slow rising edge of the output from the debouncing circuit to suit the input of the flip/flop, which doesn't like to talk directly with such unsophisticated signals.

When the Q output of IC3b (SHIFT OUT) goes High, IC9b's Set input is asserted and it forces IC9a's Reset input Low, while IC9a's Set input is pulled High. This allows clock signals to be entered into IC12 through the wired AND gate consisting of D7, D8, and R10, while the #SHIFT OUT input to IC8d prevents the IC10–IC11 latch outputs from being disabled by the #OE inputs going High.

The input of OR gate IC7c is pulled high by R18, allowing clock pulses from the internal oscillator to flow through via D9 to the clock inputs of Dual 64bit Shift Register IC4 (4517) and Dual 4bit Counter IC5 (4520). IC4's output (SHIFT DATA) is fed back to its input so that the sampled data is retained for any further display runs. This output is fed into the beginning of the output chain via D4. This input to the first IC10 data latch is usually disabled by D3 which pulls the signal down whenever the latch outputs are disabled (#OE High). As described in Part 3, the input buffer outputs have

been disabled by Q1, and the 10K pull−down resistors made unable to pull below ~0.7V, when SHIFT OUT was asserted. So with the IC10−IC11 latch outputs always active, these ICs work as one big parallel output shift register. Data is shifted one bit ahead on each internal oscillator clock cycle until counter IC5 reaches 128 and resets itself and IC3 just like in Sample Data input mode. Before this, the sequence can be paused by toggling the state of IC3b with B3, or by halting the internal oscillator by switching it to Pulse mode.

Part 9: External Output

In external output mode SW5 switches the resistors (R4a/b) on the IC10−IC11 #OE inputs away from GND to a signal controlled by an external device. Similarly, low impedance inputs to D5 and D14 override the output of IC12 at the LE inputs. The output of IC7b is High whenever SW5 is on, this holds IC9b (and in turn IC9a) in Reset, as well as IC3 and IC5. It also turns off Q3 (BC55x), allowing a Low input at the external control signal "LPT SELECT" to enable IC11's latch inputs via IC6b and D14. At the same time, an inverted LPT SELECT signal is applied to IC11's #OE input via R4b, making sure that its outputs are disabled. IC10's #OE and LE inputs are connected similarly, but without the inverters so that it is in the opposite state to IC11 and whenever one's outputs are enabled, the other is sampling its inputs. R6 and C1 make sure that when LPT SELECT changes, IC11's outputs are not enabled before the signal has propagated through IC6b and latched its inputs.

By alternating this action under the control of the external device, all sixteen inputs are able to be put across the eight bit output data bus. However a disadvantage is also present in that software not designed specifically to work with the Logic Visualiser will likely not output a suitable signal to use for LPT SELECT. The internal oscillator can not be used for this purpose, because it would not by in sync with the external device, and as such it may command the latch outputs to change state at the same moment as the external device is trying to read them, corrupting the data that it receives. The Alternative Output mode described in the next part resolves this problem.

Pin 1 of the DB25 connector ("/STROBE" on the PC parallel port) controls the LPT SELECT signal. The eight data outputs are on the parallel port data pins 2−9 in ascending order. As is the parallel port's way, Ground monopolises the bottom row, with connections on pins 18−25. The other pins are unused.

Part 10: Alternative External Output

The IC10−IC11 latch ICs are able to be configured as buffers by leaving their #OE inputs Low and their LE inputs High. However due to the

feed−forward resistors required for the Data Sampling output mode, this would result in the inputs "flowing through" to all the latches following them. To prevent this, SW1 is connected with a 200ohm pull−down resistor in parallel with R19 so that alternating inputs can be selected on the DIP switch, and these are forced low regardless of the feed−forward resistor from the previous stage. The outputs of the input buffers can source current through their series diodes, just not sink it, so feed−forward resistors connecting with a Low output will not affect them. As there is no way to multiplex the output without an input from the external device, the loss of half the input channels is no issue.

The IC10−IC11 LE inputs can be forced High by direct jumper connections with Vcc, because they are only ever pulled low via 1K resistors. The #OE inputs are already left enabled indefinitely in the sampling state of Pulse mode. It must be ensured that the input buffers connected to the unused inputs selected on SW1 never go High, because the current passed through the 200ohm pull−down resistor could damage them. This is why a dedicated cable is recommended, with all these inputs connected directly to GND.