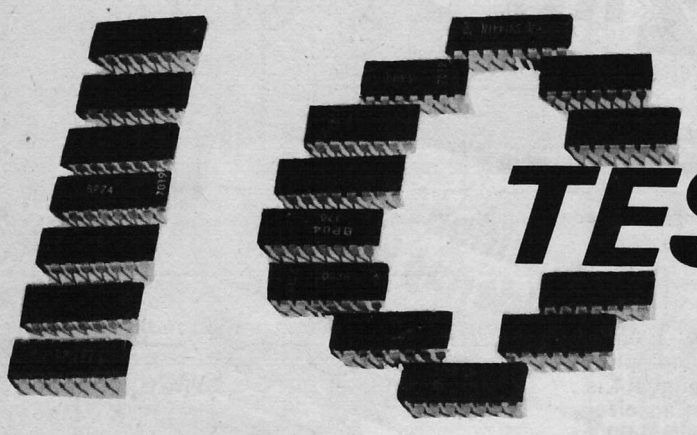
DIGITAL I.C. TESTER



By D. Burn Ph.D

Provides a rapid functional check-out for digital 'dual-in-line' integrated circuits

RECENT articles on digital integrated circuits in this magazine have stimulated a considerable interest in these fascinating devices. Added to the fact that they are now available to the amateur at low prices, many readers will doubtless wish to experiment with them.

When using transistors, particularly the low-cost bargain variety, the wise experimenter will have carried out a few simple tests on each one before incorporating it into his circuit. The same precaution is advisable to an even greater extent when using i.c.s, for trouble-shooting a complex system is difficult enough without the added complication of one or more dud i.c.s.

The tester to be described will carry out fairly simple go-no go tests on a wide variety of i.c.s., and is particularly aimed at the TTL dual-in-line series which is currently available with the largest choice of functions. However, both RTL and DTL can be checked, and simple adaptors could be devised for other types of i.c. package.

FLEXIBILITY

The major problem with an instrument of this type is to provide sufficient flexibility to enable any one of a very large range of possible logic functions to be checked, from a simple two input NAND gate to a complex four bit binary adder. The key to this problem lies in the use of patch-cords, which, although perhaps somewhat untidy, offers an economical solution.

The i.c. to be tested is plugged into a 16 pin socket, every pin of which is wired to a single pole, four-way switch. These switches enable each pin to be connected either to 0 volts, a logical 1 voltage, the supply voltage or, via a patch-cord socket, to some other input or output function.

The input is provided by a versatile pulse generator, while the output may be a voltmeter, an indicator lamp or an oscilloscope.

POWER SUPPLY

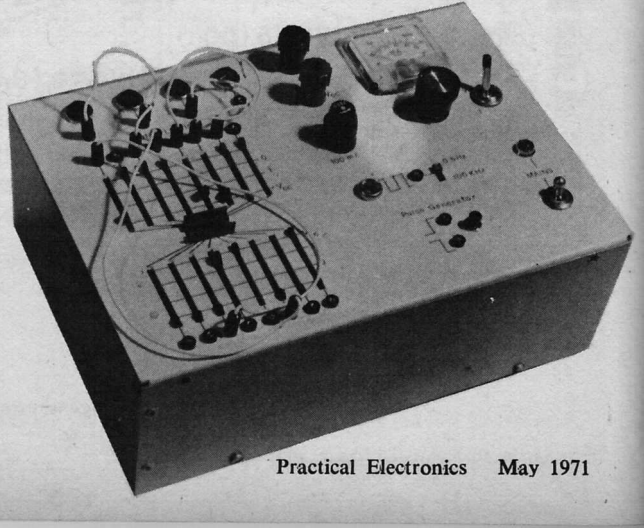
The circuit may conveniently be divided into two parts, a power supply with associated meter circuit, and a pulse generator with associated indicator lamps.

In the power supply circuit (Fig. 1) the output of transformer T1 is rectified by diodes D1 to D4, smoothed by C1 and fed to R1 and the Zener diode D5 to provide a fixed supply of 5·1 volts for the pulse generator and the indicator lamps.

Diode D6 provides a 12 volt source, part of which, selected by VR1, is fed to the base of the series transistor TR1.

The output from the emitter of TR1 is a voltage which may be varied from zero up to about 10V and forms the supply to the i.c. under test. In the prototype, a 2N3055 was used here, but it is probable that a transistor of a lower rating could be substituted.

Capacitor C3 further smooths the output, while C4 is a decoupling capacitor to prevent instability.



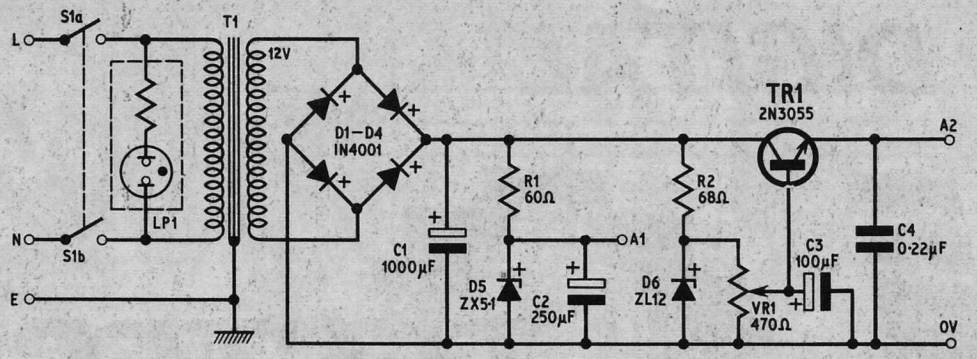


Fig. 1. Circuit diagram of power supply for the I.C. tester

METER CIRCUIT

Meter M1 (Fig. 2) is calibrated to read 0–100mA and 0–10 volts. Here a 1mA meter with a multiplier resistance R3 of about 10kΩ is used. The shunt R4 is made from a piece of resistance wire from an electric fire element. Both of these resistors should be chosen by experiment to suit the meter.

S2 is a single pole, biased, change over switch which may be either toggle or push-button. In the normally closed position, the power unit output voltage V_{CC} is read. In the normally open position, the current being drawn by the i.c. under test is metered.

Both the 0 volt and V_{CC} output are routed to take-off terminals SK1 and SK2 so that the 0 volt line is available as an earth return when an oscilloscope is being used, and the V_{CC} line is available when an external load, required by some i.c.s, has to be connected.

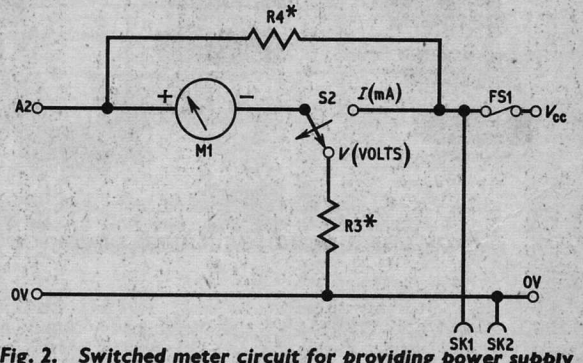


Fig. 2. Switched meter circuit for providing power supply current and voltage readings

PULSE GENERATOR

In Fig. 3, TR3 and TR4, together with their associated components, form a simple multivibrator. With switch S3 open, C5 and C8 give a frequency of about 100kHz. Closing S3 connects C7 and C6 across C5 and C8 and results in a pulse rate of about 1Hz.

Since digital i.c.s, and particularly the TTL type, require clock waveforms having rise and fall times of the order of 10 to 20nS for reliable operation, the multivibrator output is sharpened up by gates G1 and G2 of IC1, connected as a Schmitt trigger.

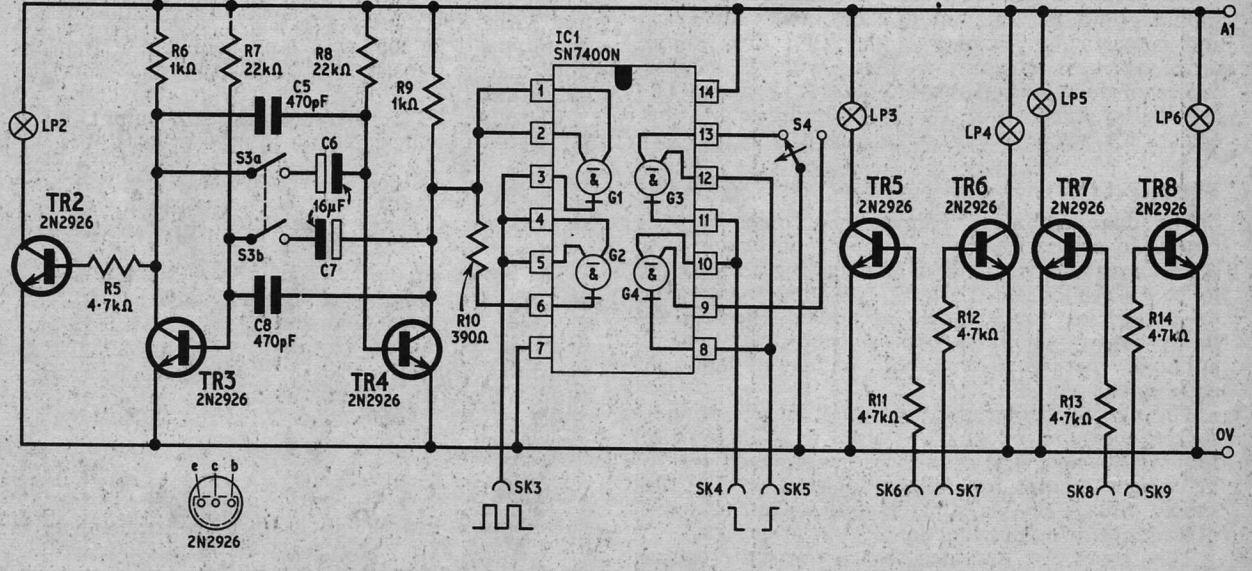


Fig. 3. Pulse generator and lamp indicator circuits

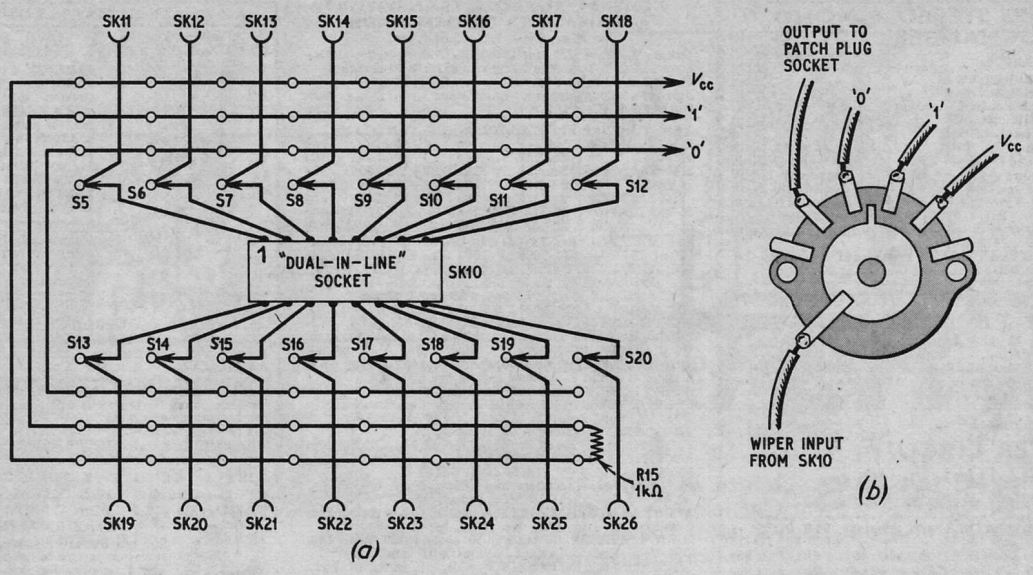
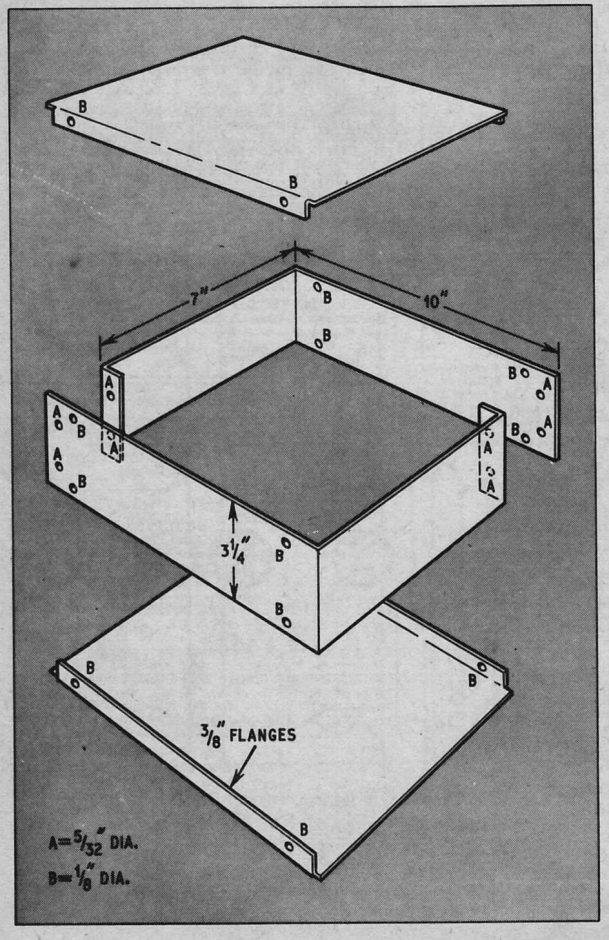


Fig. 4. (a) Wiring layout of i.c. test socket and pin switches. (b) Wiring pattern for all switch wafers. Note that only one half of the wafer is used. This figure should be consulted when assembling and wiring the switch banks

Fig. 5. Constructional details for assembling the aluminium case. Binder screws for fixing the side panels should be 2B.A. The upper and lower plates are fixed with 4B.A. screws



The wiring adopted for the pulse generator and its indicator lamp is such that the lamp LP2 follows the clock pulse, i.e. it is on when the clock is at a logical 1, but it does not load the output of the Schmitt and thus avoids possible degradation of the rise time.

The lower pulse rate allows the operation of an i.c. to be followed with the indicator lamps, while the fast pulse checks the operation of the i.c. at high speed, and is intended to be used with an oscilloscope.

The other two gates of IC1 are connected as a simple flip-flop which is used, in conjunction with the change-over switch S4, to provide single rising or falling waveforms for manual operation. This system is essential to avoid the multiple pulses that would otherwise be produced by the inevitable contact-bounce of the switch.

Four indicator lamps, LP3–LP6, and their associated amplifiers TR5–TR8, are provided for monitoring the operation of an i.c. under test. Resistors R11–R14 limit the current drawn from the i.c. output, and are wired to the patch-cord sockets SK6–SK9 so that any pin may be connected to any indicator.

The wiring of the i.c. 'dual-in-line', 16-way socket SK10, the 16 single-pole four-way switches S5–S20, and the associated patch-cord sockets SK11–SK25, is shown in Fig. 4a. Notice that the logical 1 level is derived from V_{CC} via a 1kΩ resistor R15. This ensures that the 1 level cannot exceed V_{CC}, a condition which would result in the instantaneous destruction of the i.c.

CONSTRUCTION

The instrument is built in a case measuring 10in by 7in by 3¼in. This may be constructed from 16s.w.g. aluminium following the dimensions of Fig. 5.

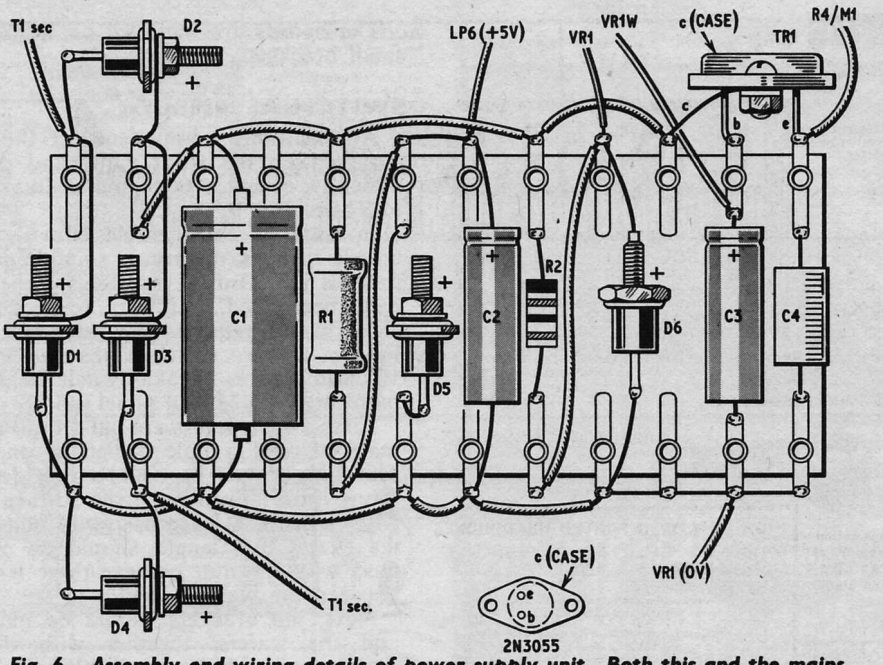
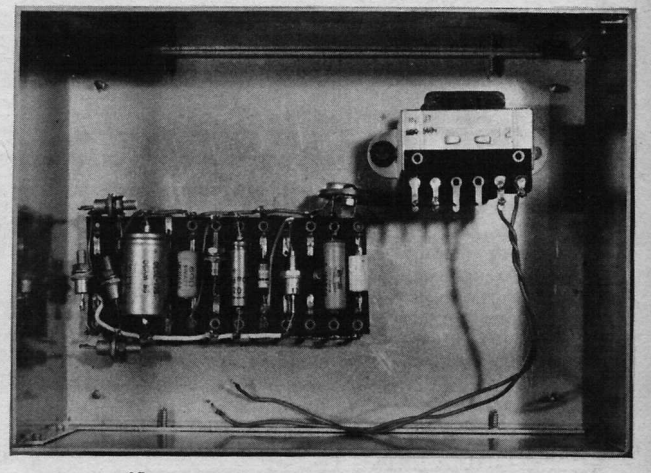


Fig. 6. Assembly and wiring details of power supply unit. Both this and the mains transformer are mounted on the chassis base plate (see photograph below)

The power unit is constructed on a 12-way piece of standard tag-board as in Fig. 6. Since TR1 is operating well within its capabilities, no heat sink is required, and it is soldered directly to the tags.

The unit is mounted on the chassis base by means of 6B.A. bolts and suitable spacers to ensure that all the components are isolated from the case. The mains transformer is also mounted on the base. The relative positioning of these units can be seen in the photograph.

The pulse generator (Fig. 7) and the lamp amplifiers (Fig. 8 and Fig. 9) are built on pieces of 0·1in matrix perforated board. Most of the wiring utilises the component leads which are passed through the board and soldered together as required.



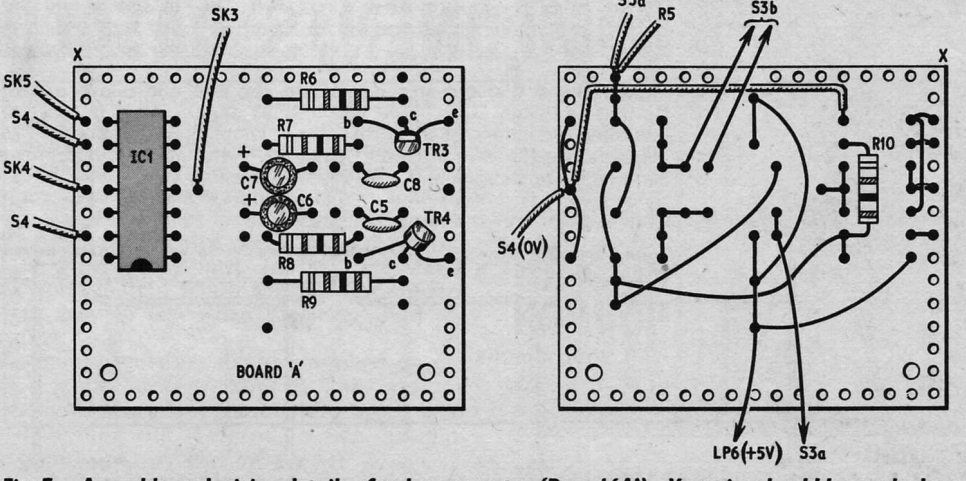


Fig. 7. Assembly and wiring details of pulse generator (Board 'A'). Veropins should be used where connecting flying leads

COMPONENTS . . .

Resistors

R1	60 Ω, 5W	R7	22k Ω
R2	68 Ω, ¼W	R8	22k Ω
R3*	See text	R9	1k Ω
R4*	See text	R10	390 Ω
R5	4·7k Ω	R11-R14	4·7k Ω (4 off)
R6	1k Ω		

All 10%, ¼ watt carbon except where stated.

Capacitors

C1	1,000μF	elect. 25V
C2	250μF	elect. 10V
C3	100μF	elect. 15V
C4	0·22μF	polyester
C5	470pF	polystyrene
C6	16μF	elect. 10V
C7	16μF	elect. 10V
C8	470pF	polystyrene

Potentiometers

VR1 470 Ω

Diodes

D1–D4 1N4001 *or* RS3OAF (4 off)
D5 ZX5·1 5·1V, 10W, Zener
D6 ZL12 12V, 1·5W Zener

Transistors

TR1 2N3055
TR2–TR8 2N2926 (G) (7 off)

Integrated Circuit

IC1 SN7400N

Switches

S1 Double pole, mains on/off
S2 S.p.c.o., biased toggle
S3 D.p.c.o., slide
S4 S.p.c.o., biased toggle
S5–S20 Double-pole, 6 way, break-before-make 'Maka-switch' wafers (Radiospares) (16 off)

Miscellaneous

T1 Mains transformer, 12V 1A Secondary, M1—1mA moving coil meter 1¾in square face, SK1, SK2 Insulated terminals, FS1—100mA fuse with panel fuseholder, LP1—Mains neon. LP2–LP6 Panel Mounting M.E.S. lamp holders with 6V, 0·06A bulbs (5 off). SK3–SK9 Miniature sockets with miniature single pin plugs to suit (9 off) (Radiospares). SK10–16 way, 'Dual-in-line' socket (Radiospares), Aluminium, 8B.A. threaded rod, washers, spacers. SK11–SK26 miniature sockets (16 off) (Radiospares).

The boards are mounted on the front panel with small brackets.

SWITCH ASSEMBLY

All the other components of the instrument are mounted on the front panel and present no great difficulty, except, that is, the 16 four-way switches S5 to S20 of Fig. 4.

In spite of considerable efforts, the author was unable to track down any suitable commercial items for this job. Ordinary wafer switches could perhaps have been used, but were rejected since a row of eight would require a panel space of some 10in. Finally, the two switch banks were constructed from 16 Radiospares 'Maka-Switch' wafers, each bank requiring only 3¾in of panel space.

First, switch levers are cut from Paxolin or similar material, and a hole drilled at one end (Fig. 10). This hole should be countersunk deeply so that the screw head is flush with the surface of the material. Also, when the lever has been bolted to the wafer, the excess bolt length should be cut off and filed flush with the nut, because there is very little space between the wafers.

Next, the brackets should be made up (Fig. 11) and the wafers, together with the washers and spacers, should be assembled on threaded rods before finally bolting the whole lot firmly together to form a rigid unit. Note that the unused tags on the side of the wafers that are towards the front panel must be bent over otherwise they will foul it.

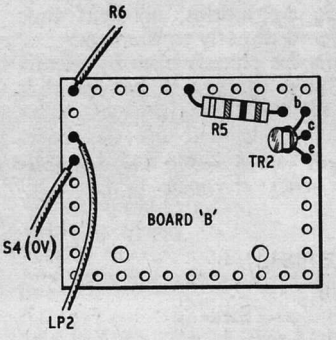


Fig. 9. Assembly and wiring detail of pulse generator lamp amplifier (Board 'B'). Clad Veroboard is used for this with none of the copper strips cut

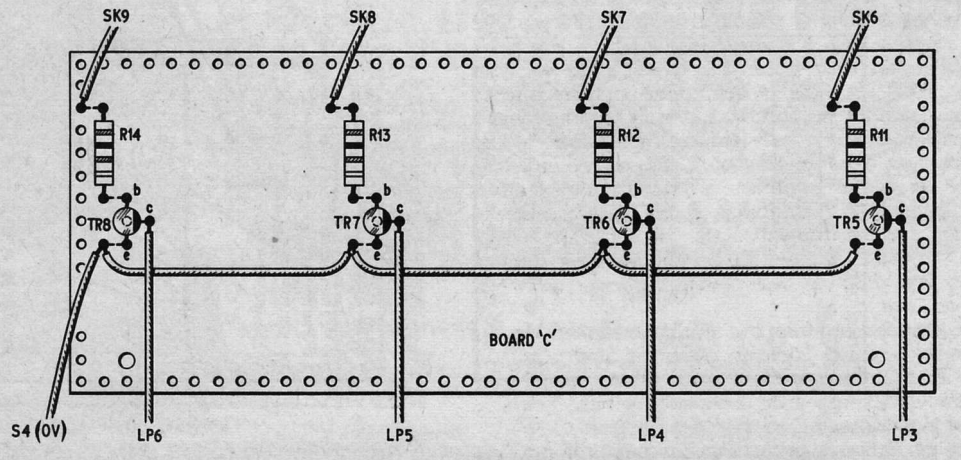


Fig. 8. Assembly and wiring details of function lamp amplifier (Board 'C')

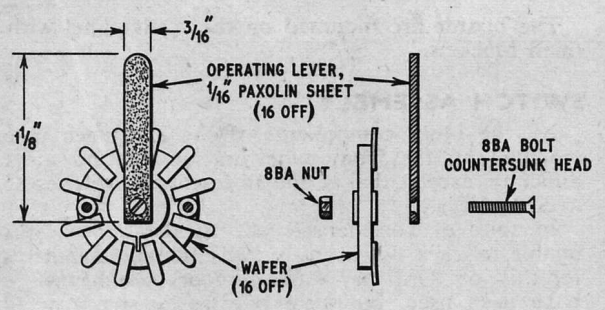


Fig. 10. Assembly details of switch levers

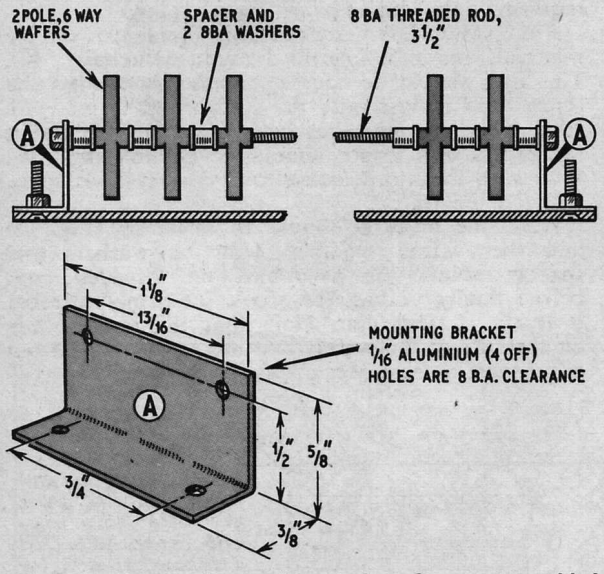
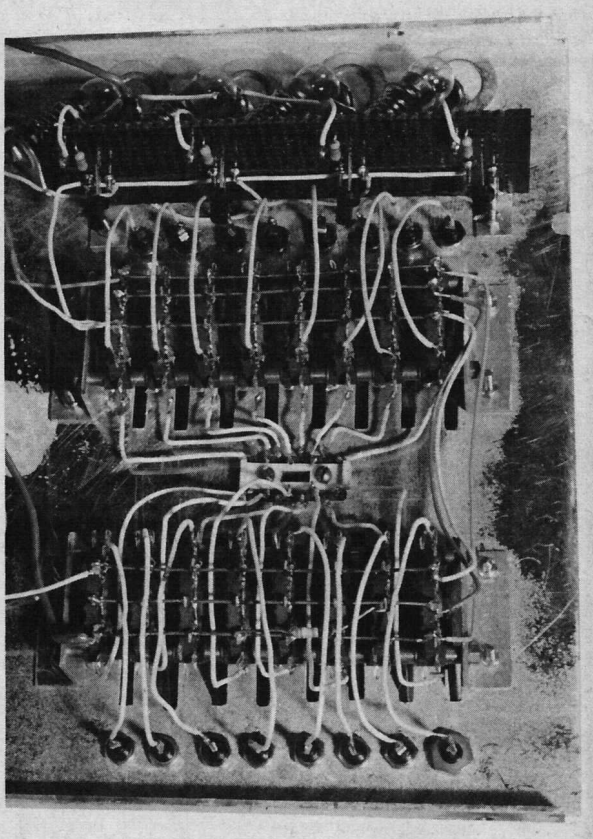


Fig. 11. Showing how eight switch wafers are assembled in a single unit. Two such banks are required



Switch banks in position. Here and in Fig. 13 some of the wafers in the lower switch banks have been reversed which accounts for asymmetric wiring. Ideally all wiring should follow the pattern of Fig. 4b. The unused underside wafer tags should be bent back to prevent chassis fouling

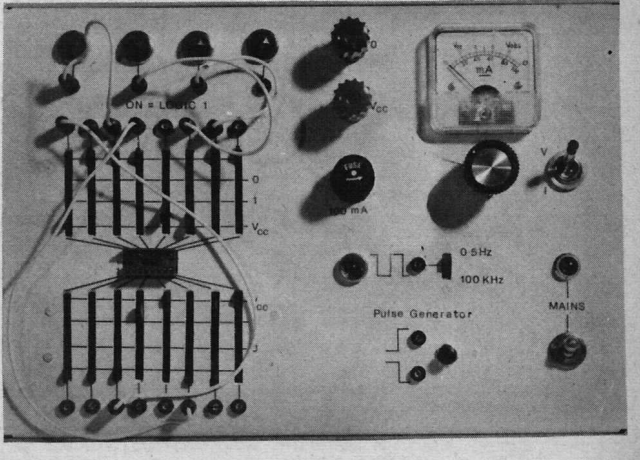
FRONT PANEL ASSEMBLY

The front panel of the case can now be cut and drilled. A suitable layout is illustrated in Fig. 12, but it is emphasised that this is not critical and may be modified to suit available components. For the same reason, drill sizes are not given, although it is recommended that the specified sockets are used for the patch-cords, in which case the holes should be 2B.A. clearance.

The only part that needs fairly accurate work is that concerned with the switch units, and the quoted dimensions should be followed closely or the switch levers may not pass freely through the slots. When the wafers are used in this way, the usual indexing employed in wafer switches is not present, and it may be thought that difficulty would be experienced in finding the correct positions. In fact, the wafer contacts are quite a tight fit on the moving contact and it is very easy to feel when the lever is in the correct position.

Before the components are finally mounted on the panel, it is a good idea to paint it and add the legends. The author used a matt white spray and added the lettering with Letraset, which gives a very neat appearance.

A coat of Letraset protective lacquer will prevent the letters being rubbed off.



The completed front panel with all the legends in position and fixed with a protective lacquer

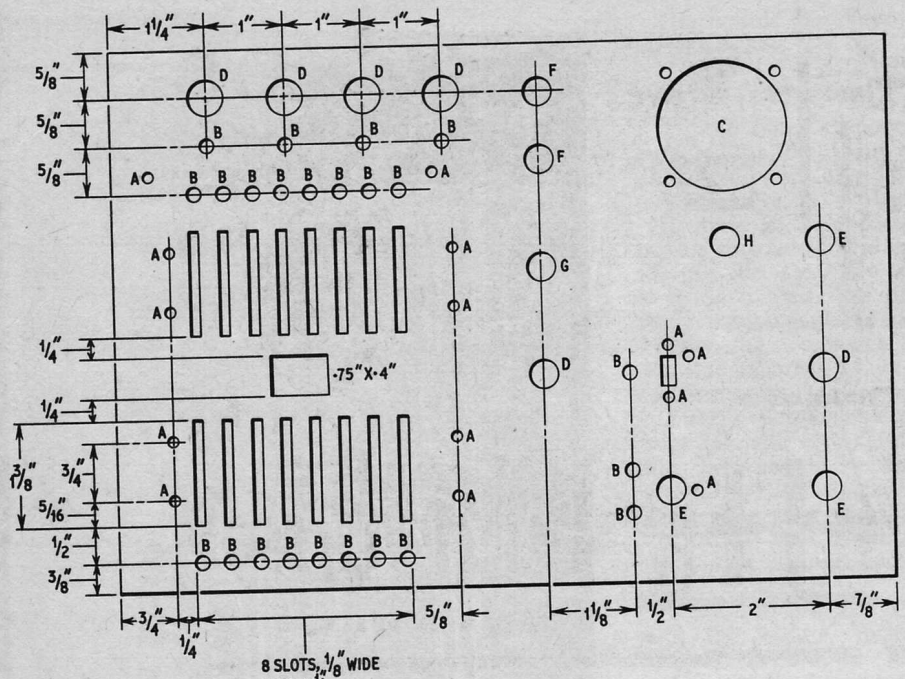


Fig. 12. Drilling details for the front panel of the tester

DRILLING DETAILS

A — 8BA Clearance
B — 2BA Clearance
C — Panel Meter
D — Panel Lamps
E — Supply Switches
F — Supply Terminals
G — Fuseholder
H — Supply Potentiometer

Holes C — H to suit components used

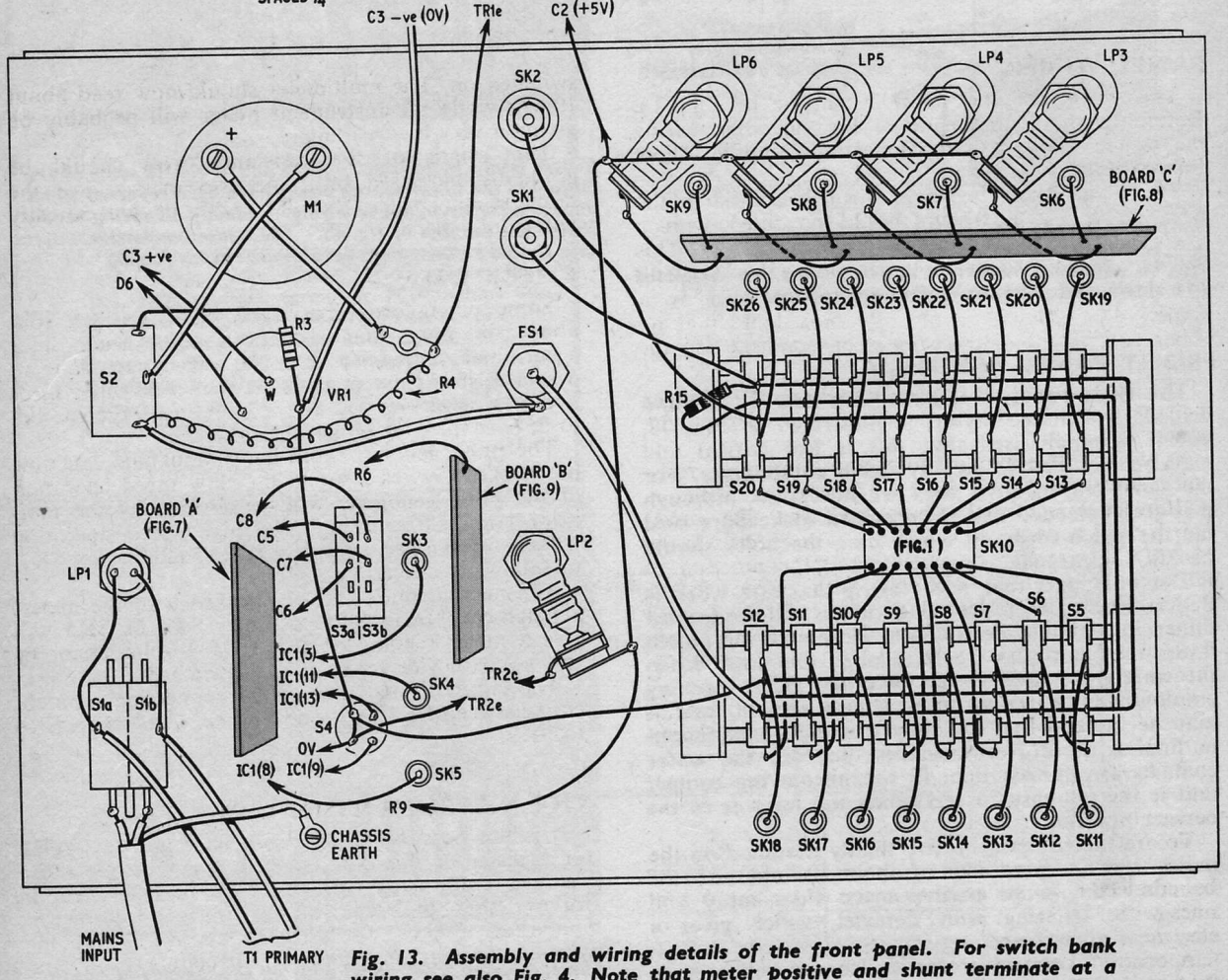
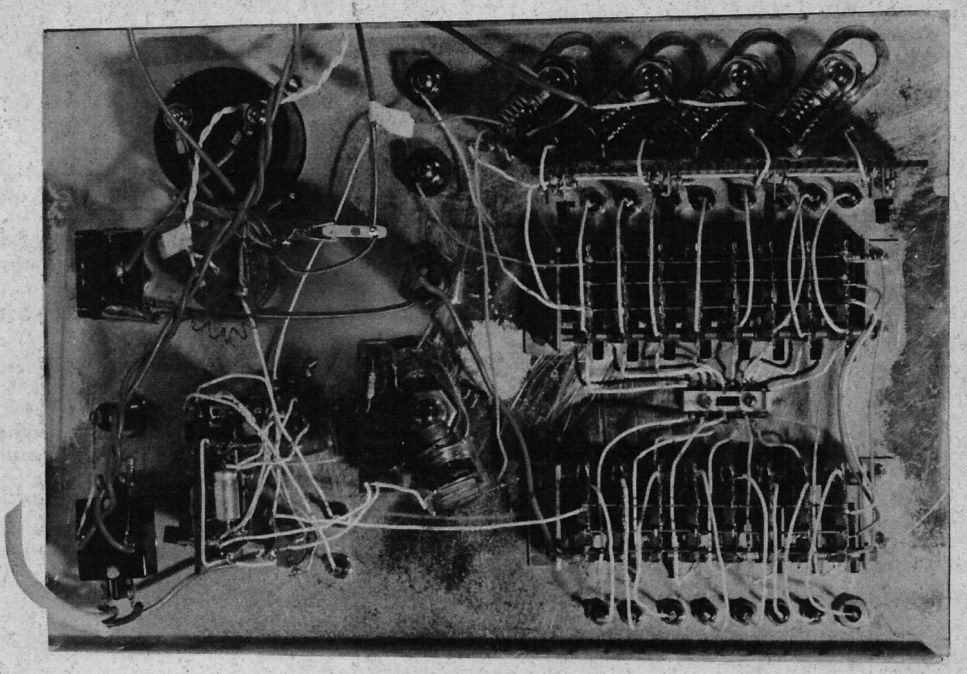


Fig. 13. Assembly and wiring details of the front panel. For switch bank wiring see also Fig. 4. Note that meter positive and shunt terminate at a stand-off insulator



PANEL WIRING

The wiring of the panel is shown in Fig. 13. Reference should be made to Fig. 4b when wiring the switch banks as all connections should follow this pattern.

The mains cable is led in through a hole in the back of the case which should be fitted with a grommet to prevent damage to the insulation. This cable is wired directly to the mains switch S1, with the earth lead being anchored to the case by a solder tag fixed with a nut and bolt. Note that no other part of the circuit should be connected to the case.

The leads from the power unit are made longer than necessary so that it is possible to work on the panel wiring.

Values of the meter shunt and multiplier resistances must be found by experiment, for which a multimeter is required. First check that the power unit is working correctly before it is connected to the rest of the circuit. The potential at the junction of R1 and D5 is about +5 volts with respect to the 0 volt line. The potential at the emitter of TR1 should next be measured, and it should vary from 0 to a maximum of some +10 volts as VR1 is turned from one extreme to the other.

Complete the wiring and connect the multimeter across V_{CC} and 0 volts. With a 10kΩ resistor temporarily wired in for R3, check that the two meters give the same reading. If the meter reads low, reduce the multiplier and vice versa, until agreement between the two meters is obtained.

To find the value of the shunt resistor R4, the multimeter and a resistor of about 500 ohms should be connected in series across the V_{CC} and 0 volt lines with V_{CC} set at about 5 volts. A short piece of electric fire element resistance wire, say 2in, is temporarily connected across the meter. S2 is switched to the current position and the unit is switched on. The multimeter should now read about 10mA, while the instrument meter will probably be giving a very low reading.

The length of the resistance wire should be gradually increased until the two meters give the same reading, then the shunt can be permanently wired into place.

CHECK OUT

Some patch-cords should be made up, say four about 3in long and six about 10in. Since it is occasionally necessary to make two connections to a socket, it is convenient to have two or three cords with a plug at one end and a loop, just large enough to fit over the plug pin, at the other.

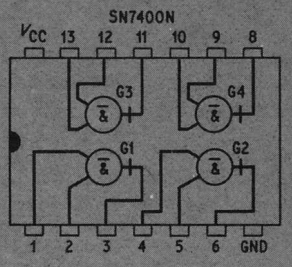
The pulse generator and lamp-amplifiers can now be checked. Switch on, and the slow speed operation of the pulse generator will be obvious by the indicator lamp LP2 pulsing. The high speed operation will require an oscilloscope, plugged into socket SK3, to follow its operation.

The manual pulse can be checked with the meter; a patch-cord from SK1 to either SK4 or SK5 will give a meter reading of about 2·5–3 volts, changing to 0 volts (or vice versa) as S4 is switched.

The lamps should turn on by connecting a patch-cord between SK1 and, one by one, the sockets SK6 to SK9.

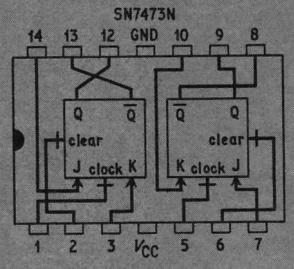
THE INSTRUMENT IN USE

It is not possible to lay down hard and fast rules for a tester of this type, since a test schedule must be devised for each type of i.c. to be examined. It follows that the type of i.c. must be known—unmarked devices are virtually useless. Once the type is known, its function, pin connections and truth table can be determined and appropriate tests worked out.



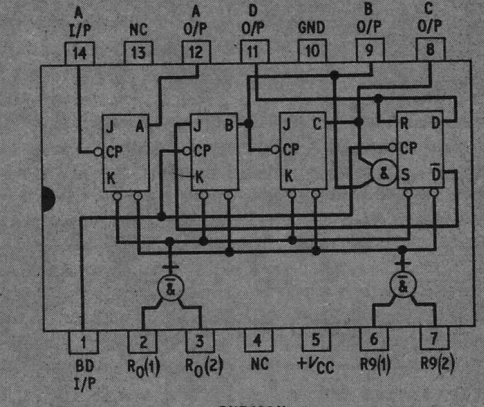
TRUTH TABLE EACH GATE		
INPUTS A	B	OUTPUT
0	0	1
1	0	1
0	1	1
1	1	0

Fig. 14. Pin diagram and truth table of a SN7400N quad two input gate. Note that this is a top view of the package



TRUTH TABLE EACH FLIP-FLOP		
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Fig. 15. Pin diagram (top view) and truth table for a SN7473N dual J-K flip-flop



SN7490N

COUNT	OUTPUTS A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

(a)

COUNT	OUTPUTS B	C	D
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1

(b)

COUNT	OUTPUTS A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0

(c)

Fig. 16. Pin diagram (top view) and truth tables for an SN7490N decade counter

It is a wise precaution first to ensure that there is no internal short circuit across the supply pins. To do this, the device should be plugged into the test socket SK10, the appropriate pin switches set to 0 and V_{cc}, and the supply voltage increased slowly from 0 while monitoring the current. If all is well, the test can proceed.

To illustrate the method of use, detailed test procedures for three TTL devices from the currently available range will be given.

QUAD TWO-INPUT GATE

The pin diagram of a SN7400N quad two-input gate and truth table are shown in Fig. 14.

First set pin switch S11 (i.e. pin 7 of the i.c.) to 0 and S13 (pin 14) to V_{CC}. Check for a short circuit. Set all gate inputs to 0, that is, S5, 6, 8, 9, 14, 15, 17 and 18, and connect a patch-cord from the output of gate 1 (SK13) to one of the indicator lamps.

It is a wise precaution in this, and all other tests, to start with all the switches in the outside position, and only move those where a pin is to be connected to 0, logic 1, or V_{CC}. This will ensure that no pin will have the wrong voltage applied to it, and that when a patch-cord is used, it will automatically be connected to the corresponding i.c. pin.

To continue with the testing of gate 1, pin switches S5 and S6 should now be operated so as to apply 0/0, 0/1, 1/0 and 1/1 levels in turn to its inputs, pins 1 and 2. The truth table tells us that the lamp should remain on for the first three pairs of inputs, and turn off at the fourth. If any other response is observed, then the gate is faulty.

Now move the patch-cord to the outputs of the other three gates in turn and repeat the procedure with the appropriate input switches. Of course, should one or more of the gates prove to be faulty, it does not mean that the i.c. has to be discarded, for the other gates can still be used.

It is a good idea to cut off the pins of any faulty gates to make sure that they are not accidentally wired into a circuit.

The tester may also be used to demonstrate some possible applications of these gates. For example, if one of the inputs to a gate is connected by a patch-cord to SK3 of the pulse generator, it can be shown that the gate will pass the clock pulses when its other input is at 1, but will block them if it is at 0.

It will also be noticed that the clock pulses are inverted by this arrangement, and that by connecting the output of this gate by a patch-cord to both the inputs of another gate, the output of the second gate follows exactly the clock pulse.

DUAL J-K FLIP-FLOP

The pin diagram and truth table for an SN7473N, dual J-K flip-flop are shown in Fig. 15.

Set the pin switch S16 to 0 and S8 to V_{CC} and carry out the usual short circuit test. Before testing of this and related flip-flops can begin, it is important to note that the truth table only applies if the clear (and preset, if present) input is at a logical 1. The clear input overrides all others, and if it is at 0, the Q output will be forced to 0, irrespective of the states of any other input. Thus S6 and S10 should first be set to 1.

Set J and K (S13 and 7) to 0 and connect a patch cord from SK11 to SK4 of the pulse generator.

Line 1 of the truth table tells us that if J and K are both 0, the flip-flop does not change state on receipt of a clock pulse, so that operating S4 will simply leave the output in its initial form.

It is perhaps helpful to connect both the Q (SK21) and the $\overline{Q}$ (SK20) outputs to the indicator lamps and verify that they are always in opposite states.

Moving to the second line of the truth table, set K to 1 and operate S4. Whatever its initial state, Q should now go to 0, and remain there for subsequent clock pulses. Set J to 1 and K to 0 and verify that Q now goes to 1 and stays there (line 3).

Finally, set both J and K to 1; line 4 tells us that after a clock pulse, Q will be in the state opposite to that before the clock pulse, in other words, the flip-flop will divide by two. The second flip-flop should now be checked in exactly the same way.

As with the SN7400N, we can also demonstrate a simple application of the SN7473N. Set J and K of both flip-flops to 1; connect a patch-cord from the Q output (SK21) of the first to the clock input of the second (SK15), and one from the pulse generator (SK3) to the clock input of the first (SK11). The combination will now divide by four, and an indicator connected to the Q output of the second flip-flop (SK24) will turn on once for every four clock pulses.

If a double beam oscilloscope is available, this can also be demonstrated at the fast pulse rate by connecting one beam to the pulse generator, and the other to the output of the second flip-flop. The 0 volt terminal should be used for the earth return to the oscilloscope.

DECADE COUNTER

The SN7490N decade counter is included as an example of medium scale integration, that is, a device containing several individual circuits interconnected so as to carry out a complex function, all in one package.

In the case of the SN7490N, four flip-flops and some additional gating are wired so as to provide a complete decade counter, with the full binary coded decimal count available at its outputs. In order to increase its versatility further, the counter is in two parts, a divide by two and a divide by five section, which may either be used separately or externally connected for use as a divide by ten unit.

The pin connections and truth tables are shown in Fig. 16, and each mode of operation will be checked in turn.

First, set S9 to V_{CC}, S17 to 0 and carry out the short circuit check. Install patch-cords from the four outputs to the indicator lamps so that the A output (SK21) goes to the left-hand lamp, the B output (SK24) goes to the next and so on—the lamps now correspond to the order shown in the truth tables.

The counter has two reset modes, each one having two AND-gated inputs. To reset the counter to 0, both the R_0 inputs must be at a logical 1, so if S6 and S7 are set to 1, none of the lamps should be on.

The counter may also be reset to binary nine, i.e. 1001, so if both S10 and S11 are set to 1, the first and last lamps should be on.

As in the case of the J-K flip-flop, these reset inputs override all others so that the truth tables will only be followed if at least one of each pair of rest inputs is at a logical 0. The two sections of the SN7490N will now be checked individually.

TWO SECTION CHECK

By connecting a patch-cord from SK5 of the pulse generator to the A input (SK19), the A output should change state once for every two input pulses. Change the input pulse to the BD input (SK11) and the B, C, and D lamps should now follow the truth table of Fig. 16b, that is, the D output gives one pulse for every five input pulses.

In order to check the full decade count, the A output must be connected to the BD input, and input pulses applied to the A input; the counter should now follow the truth table shown in Fig. 16a. It can be seen that the D output provides 1 output pulse for every ten input pulses.

The usefulness of the two-gated reset inputs may be demonstrated in the following way. Install patch-cords from the B and C outputs (SK24 and 25) to the R_0 inputs (SW12 and 13), the remaining connections being as for the decade count. Now when the count reaches six, i.e. binary 0110, both reset inputs will be at 1 and therefore force the counter to reset to 0, skipping the rest of the decade count sequence.

This is shown in the truth table of Fig. 16c, from which it can be seen that a divide by six function is available at the B or C outputs.

Other division ratios may also be obtained on the same way, providing the required ratio does not have more than two 1's in its binary number.

The above examples have shown how a test schedule may be devised for any one of three widely different types of TTL i.c. Using the same techniques, the reader may readily devise suitable tests for any of the currently available TTl devices, and with only minor modifications, devices of the RTL and DTL ranges. ★