CHIP CHECKER

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THIS device differs from most i.c. testers in as much that the logic states of all the i.c. pins can be seen at a glance. Not only are the high and low states displayed, but this checker differentiates between high, low, inadmissible, and open circuit states.

Although the tester does not check *all* the different aspects of a logic i.c. it does allow go/no-go devices to be identified quickly and can, with practice, go a long way to identifying an unknown i.c.

The circuit design allows the use of cheap calculator type multiplexed displays.

OPERATION

The operation of the device is basically simple and consists of a set of three comparators which are very rapidly switched around the pins of the i.c. under test, whilst at the same time enabling the appropriate display digit.

CD4016 quad analogue switches i.c.'s 1 to 4 are employed to switch the comparators onto each pin.

The switching sequence is controlled by a four to sixteen line decoder (IC5) which operates the switch controls and also enables the digit drivers (IC's 7, 8 &9).

The decoder is fed by a binary counter IC6 which is in turn clocked by a 500Hz oscillator made up from two of the gates in IC12.

Interdigit blanking is necessary and is achieved by feeding clock pulses from the oscillator, after inversion by TR2, to the blanking input of the binary to seven segment decoder IC13. This ensures that all displays are off during the first half of the clock pulse.

COMPARATORS

IC10 (LM324) is a quad op-amp and three of the four amplifiers in the package are used as comparators to detect the logic state of the pin being sampled.

Logic "1" is detected by IC10c, the output of which goes high if a voltage greater than +2·4 volts is present at its input.

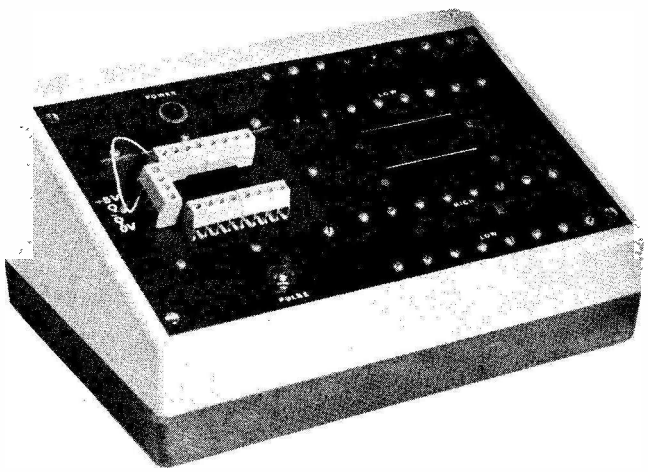
Logic "0" The outputs of all three comparators are arranged to be low when a voltage between 0 and +0·4 volts is present on the inputs.

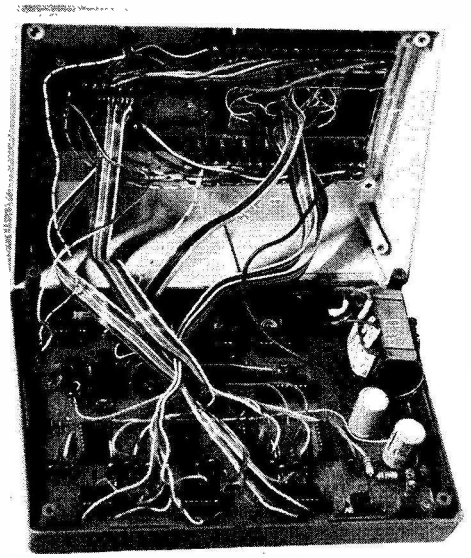
Inadmissable levels (+0·4 volts to +2·4 volts) are detected by IC10a. The output is high when a voltage greater than +0·4 volts is present on its input.

Open circuit Any pin that is open circuit either by design or a fault condition is detected by IC10b.

A negative voltage is fed onto each test pin by means of 1MΩ resistors 1-16, and clamped by germanium diodes D1-16 to approximately −0·2 volts. When an i.c. is plugged into the test socket this small negative voltage, when connected to a live pin, will be clamped to zero or overridden by the positive voltage present on that pin, provided of course that the supply is connected to the i.c. under test by means of the terminals provided.

IC10b detects the presence or absence of this negative voltage, and if present its output goes high, the output from the gating circuitry presents a binary code greater than nine to the decoder IC13 and it automatically blanks the display. Any other condition causes IC10b to produce a low output, leaving the display format to be decided by the other two comparators.





COMPONENTS . . .

Resistors

R1-R16, R32	1M $\frac{1}{8}$W (17 off)
R17-R19, R21, R22, R33	100k $\frac{1}{8}$W (6 off)
R20, R23, R34, R54	10k $\frac{1}{8}$W (4 off)
R56, R24	22k $\frac{1}{8}$W (2 off)
R57	6M8 $\frac{1}{8}$W (1 off)
R25-R31	150 $\frac{1}{8}$W (7 off)
R51, R52, R55	1k $\frac{1}{4}$W (3 off)
R35-R50	2k7 $\frac{1}{4}$W (16 off)
R53	330 $\frac{1}{4}$W (1 off)

Potentiometers

VR1, VR2, VR3	47k min. preset
VR4	100k min. preset

Capacitors

C1	10n Disc Cer.
C2	1µ Tant.
C3, C9	47.0µ elect. 15VDC (2 off)
C4, C5, C7, C10	100n 30V Disc Cer. (4 off)
C6, C8, C11	100µ 16V Tant (3 off)
C12	22µ 16V elect. (1 off)

Transistors

TR1, TR2	BC107 (or similar) (2 off)

Diodes

D1-D16, D29	OA90/91 (gen. purp. germanium) (17 off)
D17-D23	IN914 (or similar) (7 off)
D24-D25	IN4001 (or similar) (2 off)
D26-D27	6·8V Zener 400mW (2 off)
D28	0·2 in. l.e.d. (green) & holder

Integrated Circuits

IC1-IC4	4016 or 4066 (4 off)
IC5	4514
IC6	4516
IC7-IC9	75492 (3 off)
IC10	LM324
IC11, IC12	4011 (2 off)
IC13	4511
IC14	74121 optional
IC15	7805

Switches

S1-S16 3-way centre-off slide switch (16 off) (Progressive Radio)
S17 Single or double pole 250V ac 1A toggle (1 off)
S18 Push-to-make switch (optional)

Miscellaneous

14-pin d.i.l. i.c. sockets (11 off)
16-pin d.i.l. i.c. sockets (3 off)
24-pin d.i.l. i.c. sockets (1 off)
T1. mains transformer 6·3V 1A
Displays. Bowmar 8 or 9 digit, or NSA 1298 (2 off) (Henrys Radio) These are common cathode
1½ Metres 8-way ribbon cable
Printed circuit board
2-core ,mains cable
Vero case 2523E
Terminal blocks Electrovalue type 7204 4-way (5 off)

DISPLAY FORMAT

The outputs from the comparators are gated by IC's 11 and 12, TR1 and D21, D22 and D23, to produce the following display characters:—

Logic "1" —displays "1"
Logic "0"—displays "0"
Inadmissable—displays "8" flashing at 2Hz.
Open circuit—displays *blank*

The fourth op-amp in the LM324 package is used as an astable oscillator running at 2Hz. By feeding this into the gating arrangements it causes the "8" to flash at 2Hz.

PULSE GENERATOR

A 74121 monostable (IC14) is provided on board to provide a clock pulse for checking counters. The Q and $\overline{Q}$ outputs are brought out to a terminal block near the test socket. The monostable is triggered by means of a push button switch, S18 mounted on the front panel. This part of the circuit may be omitted if not required.

POWER SUPPLY

The power supply consists of a 6·3 volt mains transformer feeding two rectifiers D24 and D25 which together with the reservior capacitors C7 and C9 provide positive and negative rails of approximately 9 volts each. A split supply is provided from the op-amp package of ±6·8V, Zener stabilised by D26 and D27.

The output voltage of the op-amps is 1·5 volts less than the supply at maximum and a further 0·6 volts is dropped by the isolation diodes, D17, 18, 19, 22 and 23, which are in series with the op-amp outputs. The total voltage loss is therefore approximately 2 volts. In order to ensure that the 5 volt logic circuitry interprets a high output from the op-amps as logic "1" the supply rail for the amplifier package needs to be 2 volts above the 5 volt supply, hence the 6·8 volts.

The 5 volt logic supply and the supply for the i.c. under test is provided by a 7805 i.c. regulator from the raw 9 volt supply, IC15.

The use of a 7805 in this situation provides a double benefit because apart from providing good regulation, should one inadvertantly switch a test pin down to chassis whilst it is connected as a supply pin, the 7805 shuts down and restores power when the short is removed, suffering no ill effects and with no damage to the offending switch.

A power indicator l.e.d. is fitted (D28), mainly to help avoid an i.c. being inserted with power on, which could result in damage to the i.c. The indicator also reduces the risk of leaving the tester switched on when not in use, which could all too easily happen if all switches were set to the centre position and the test socket unoccupied, leaving a totally blank display.

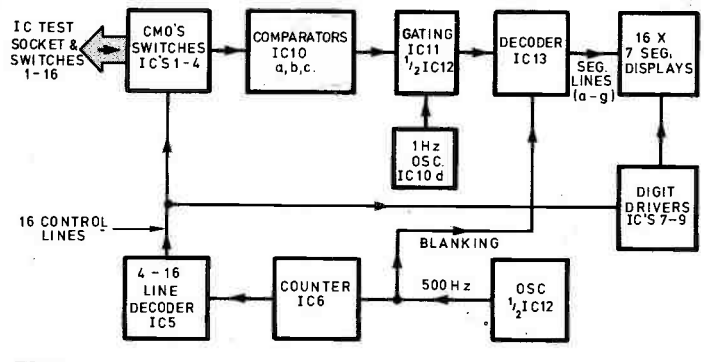


Fig. 1. Block diagram of Chip Checker

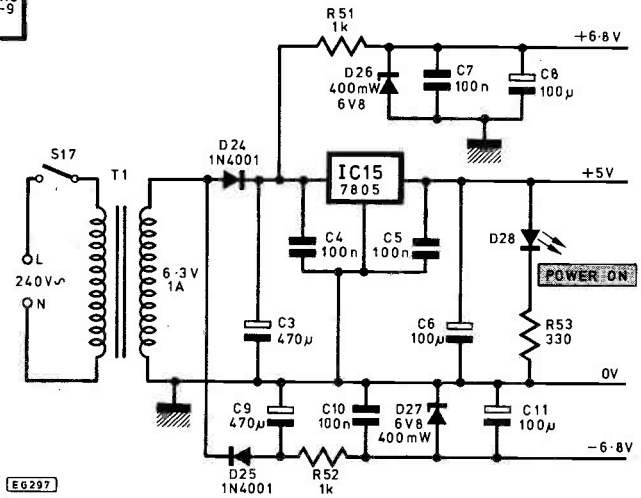


Fig. 2. Power supply

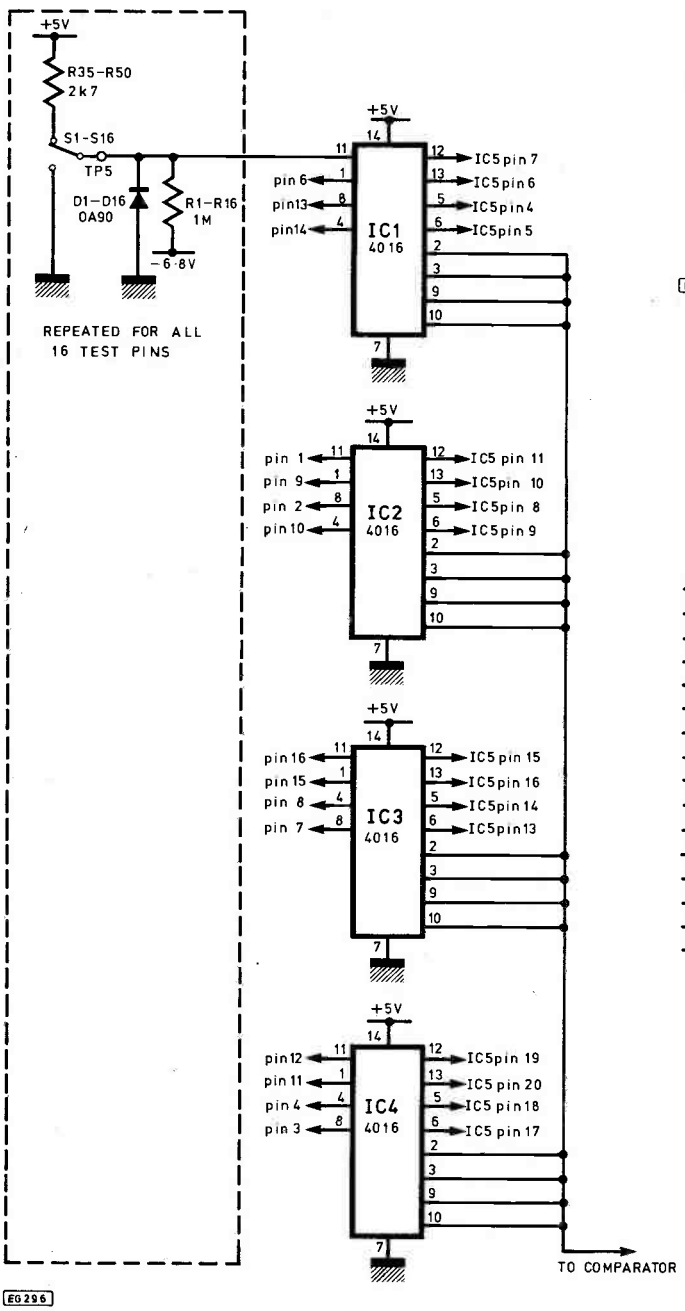


Fig. 3. CMOS switching stage

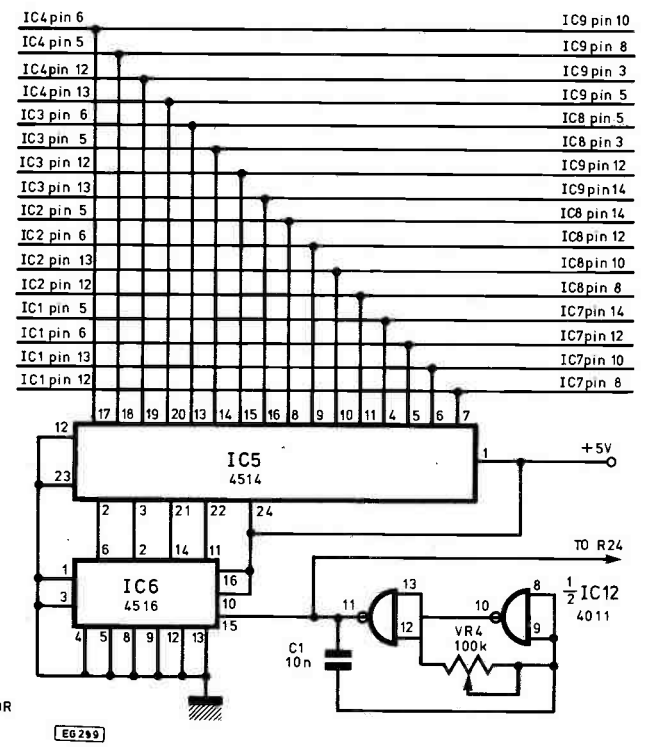


Fig. 4. Clock, and switch sequence control

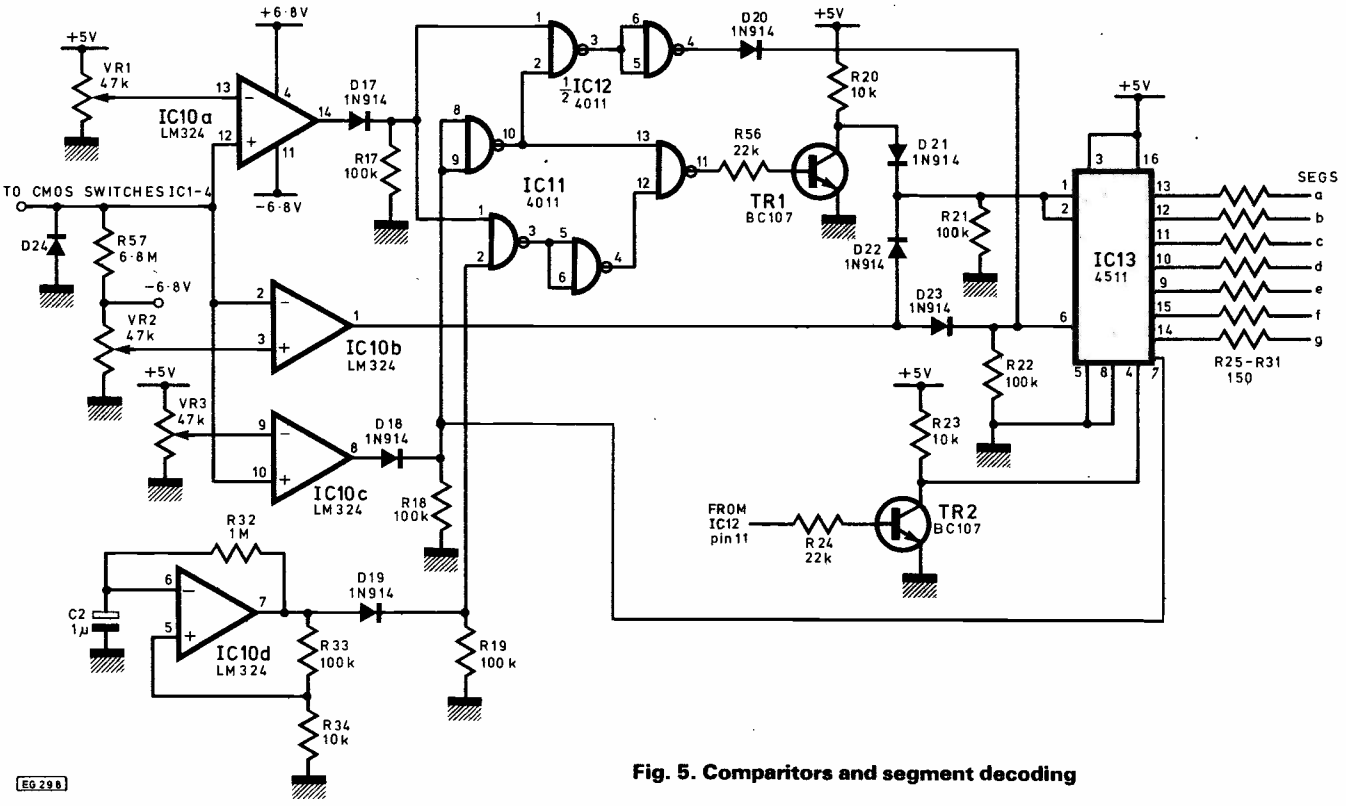


Fig. 5. Comparitors and segment decoding

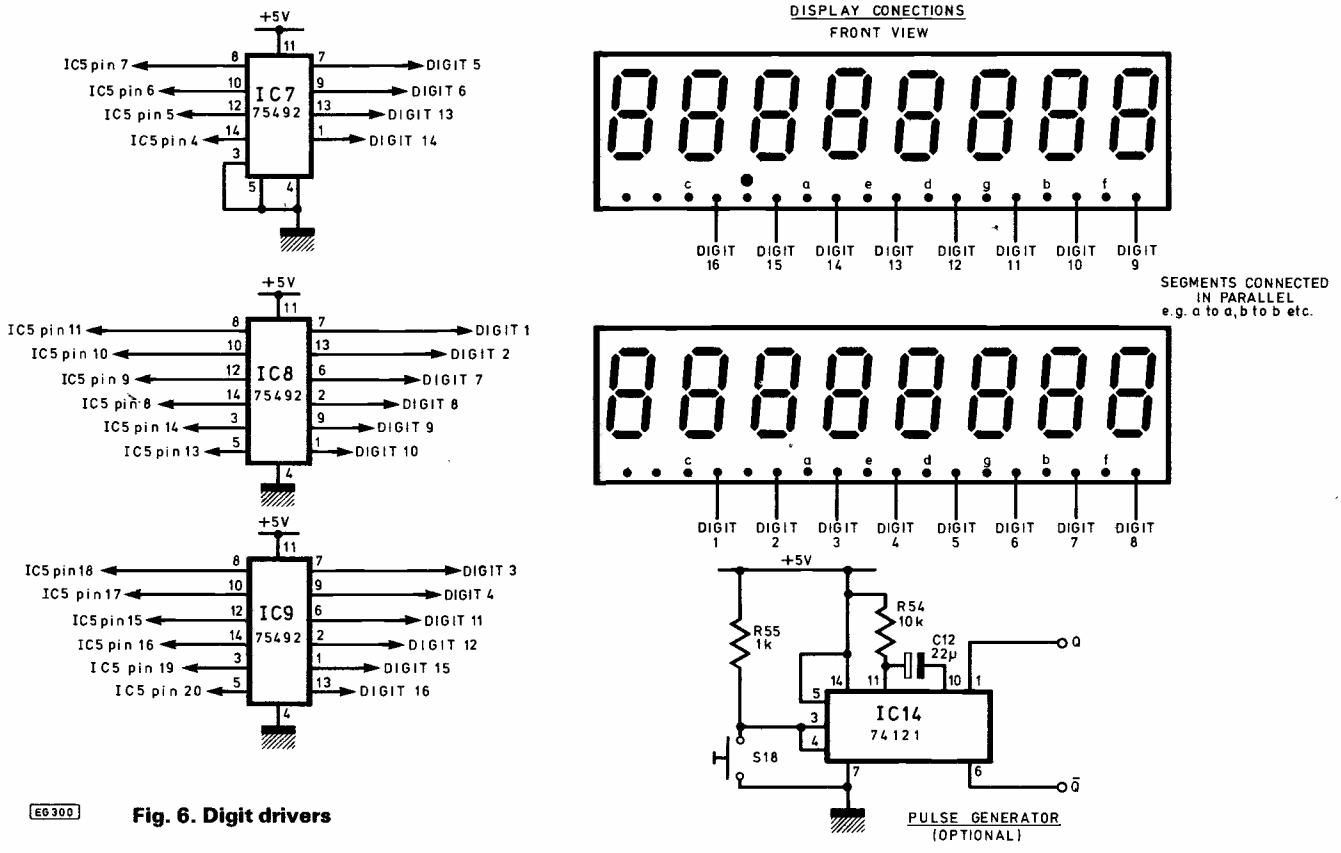


Fig. 6. Digit drivers

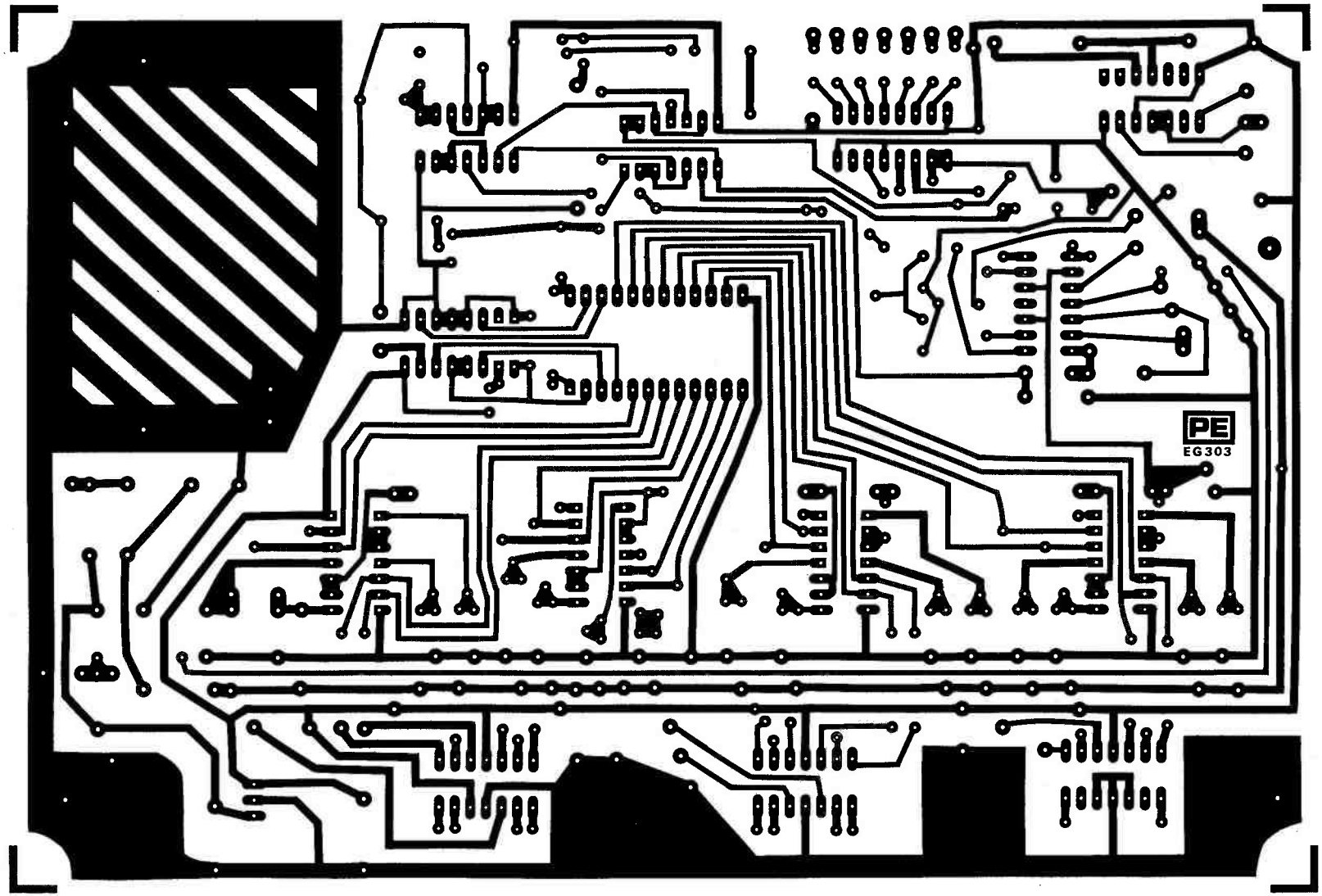


Fig. 7. Printed circuit layout (actual size)

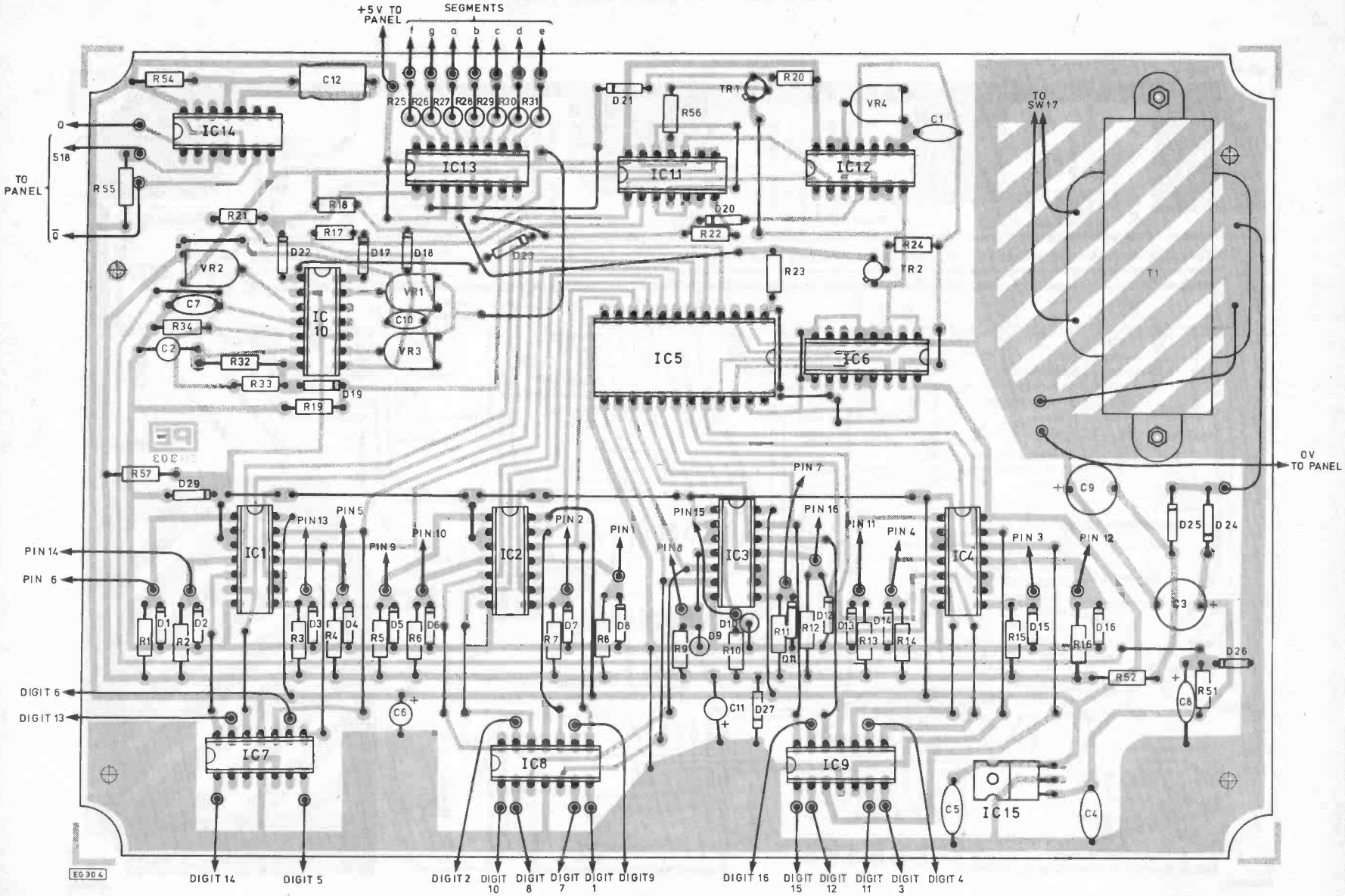


Fig. 8. Component layout

The +5 volts rail and the ground rail are brought out to terminals on the front panel to power the i.c. under test, and for external use if required.

The +5 volts is connected to the i.c. under test by means of a wire link connected to the +5V terminal and the appropriate supply pin on the test socket. The ground connection is made by switching the appropriate switch low.

TEST SOCKET

The test socket, apart from being wired to screw terminals, is also wired to a set of sixteen switches, S1-16, which allow any one pin to be set high, low or floating. In high position +5 volt is applied to the pins by 2k7 pull up resistors (R35-50), which allow open collector devices to be tested, and prevent smoke being produced by the device under test if two inputs are short circuit.

CONSTRUCTION

The layout is in no way critical and should present no problems to anyone wishing to use a different form of construction.

If the printed circuit layout is used it may help to fit all the jumper wires first, using sleeving if required. This avoids missing and jumpers due to the position being obscured by other components.

Before fitting any i.c.s, check that the negative voltage on the cathodes of the clamp diodes D1-16 and D24 is −0·2 volts or less. Any voltage greater than −0·2 volts will cause the 4016 i.c.s to fail. The various supply rails should also be checked at this point.

When fitting the i.c.s, make sure the power is off, and check orientation very carefully.

Ribbon cable is strongly recommended for connections between the front panel and the main board; it makes for a much easier time during assembly and fault finding if necessary.

SETTING UP

(1) Set all front panel switches to the centre position.
(2) Set all four presets to mid position. Displays should now be active.
(3) Adjust VR2 until displays are just off.
(4) Switch off and connect a 1K or 5K potentiometer across the +5 volt supply with the wiper to any test pin terminal. Connect a meter between wiper and zero volts. Switch on.
(5) Adjust the pot. for a reading of +2·4 volts on the meter and adjust VR3 until display just reads "1".
(6) Reset the pot. for a reading of +0·4 volts on the meter and adjust VR1 until display just reads "0".
(7) Rotate the pot. from one end to the other and check that the display reads "0" at one end, "flashing 8" around the centre and "1" at the other end. If this does not happen you have a fault.
(8) Disconnect pot. and meter and set all front panel switches to the low position one at a time, and check that the digit applicable to that switch reads "0".
(9) With all switches set low adjust VR4 for minimum flicker on the displays.
(10) Set all front panel switches high and check the appropriate display reads "1".

Returning all switches to centre should leave display totally blank.

USING THE CHIP CHECKER

When a TTL or DTL i.c. is plugged in and the power supply connected, if all switches are placed in the floating position, the open circuit pins if there are any, will be blank. The output pins will display one or zero and of course so will the supply pins. The input pins will normally adopt an inadmissible level of approximately +1·4 volts. The input pins will be obvious due to the flashing 8 displays. The switches may be used to program the inputs whilst the outputs can be observed on the displays and correct or faulty operation ascertained.

Counters may be clocked using the push button and monostable arrangement and the outputs all monitored at once.

If an *unknown* i.c. is plugged in, the power supply pins may sometimes be found by leaving all switches in the floating position and applying +5V only to each pin in turn and noting the number of ones present on the display. The supply pins produce the largest number of ones, thus the two pins that produce the same number as well as the larger number, may normally be assumed to be the supply pins. The polarity can then be determined with an ohmmeter.

If the supplies are then connected, the inputs will be visible by the presence of the inadmissible logic levels. The inputs can now be systematically programmed high or low, the outputs monitored and a truth table made up.

The ability of Chip Checker to detect an open circuit pin is useful when testing tri-state devices, a disabled tri-state output should behave as an open circuit and produce a blank display digit.

It should be noted that input pins can interact with one another if left floating and so all pins that need to be high should be switched high and not left floating. A short circuit between two inputs or adjacent pins will be obvious, when one is taken low by a switch the other will indicate low also even though it is switched high.

Chip Checker was primarily designed to test TTL i.c.s. EG 74L, 74S, 74LS, and of course standard 74 series. It will however handle DTL and CMOS i.c.s although the input pins of CMOS will produce blank displays due to the very high input impedance of these devices, and of course the logic levels are incorrect for CMOS. DTL i.c.s behave similar to 74 series.

Since the tester was first built it has been used for checking untested "fall out" devices and the monitor ROM's of an MK14, also buffers and gates from home computer systems after those inevitable accidents that occur during system expansion and modification.

The device has proved both reliable, and with a little practice, easy to use. ★